GigaDevice Semiconductor Inc.

GD32M531xx
Arm® Cortex®-M33 32-bit MCU

Datasheet

Revision 1.0

(Mar. 2026)

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1. General description

The GD32M531xx device belongs to the home appliance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M33 core. The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The processor is based on the ARMv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP.

The GD32M531xx device incorporates the Arm® Cortex®-M33 32-bit processor core operating at 180 MHz frequency. Flash accesses 0~6 waiting times to obtain maximum efficiency. It provides up to 320 KB (256KB main flash / 64KB data flash) of on-chip Flash memory, 32KB SRAM memory. Both FLASH and SRAM have ECC capabilities. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to two 12-bit successive approximation ADCs, two advanced timers, four general timers, three compare timers as well as standard and advanced communication interfaces: An I2C, four UARTs, a SPI, a CAN. Additional peripherals as trigonometric math unit (TMU), and space vector pulse width modulation (SVPWM) are included.

The device operates from a 2.7V to 5.5V power supply and available in –40 to +105 °C temperature range for grade 7 devices. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32M531xx devices focusing on the application field of air conditioning outdoor units.

2. Device overview

2.1. Device information

Table 2-1. GD32M531xx devices features and peripheral list

Part Number		GD32M531xx					
		CB	CZ	CC	RB	RZ	RC
FLASH (KB)	Main area	128	192	256	128	192	256
	Data area	64	64	64	64	64	64
	Total	192	256	320	192	256	320
SRAM (KB)		32	32	32	32	32	32
	Advanced timer(16-bit)(1)	2	2	2	2	2	2
	General timer (16-bit)(2)	4	4	4	4	4	4
	Compare timer (16-bit)(3)	3	3	3	3	3	3
	SysTick	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2
Connectivity	UART	4	4	4	4	4	4
	I2C	1	1	1	1	1	1
	SPI	1	1	1	1	1	1
	CAN	1	1	1	1	1	1
12bit ADC	Units	2	2	2	2	2	2
	Channels	10	10	10	16	16	16
DAC	Units				1	1	1
	Channels				2	2	2
CMP		4	4	4	4	4	4
Tsensor		1	1	1	1	1	1
TMU		1	1	1	1	1	1
GPIO		39	39	39	53	53	53
Package		LQFP48			LQFP64		

Notes:

(1) Advanced timer (AD TM) includes: TIMER0, TIMER7 (16bit x 8ch)

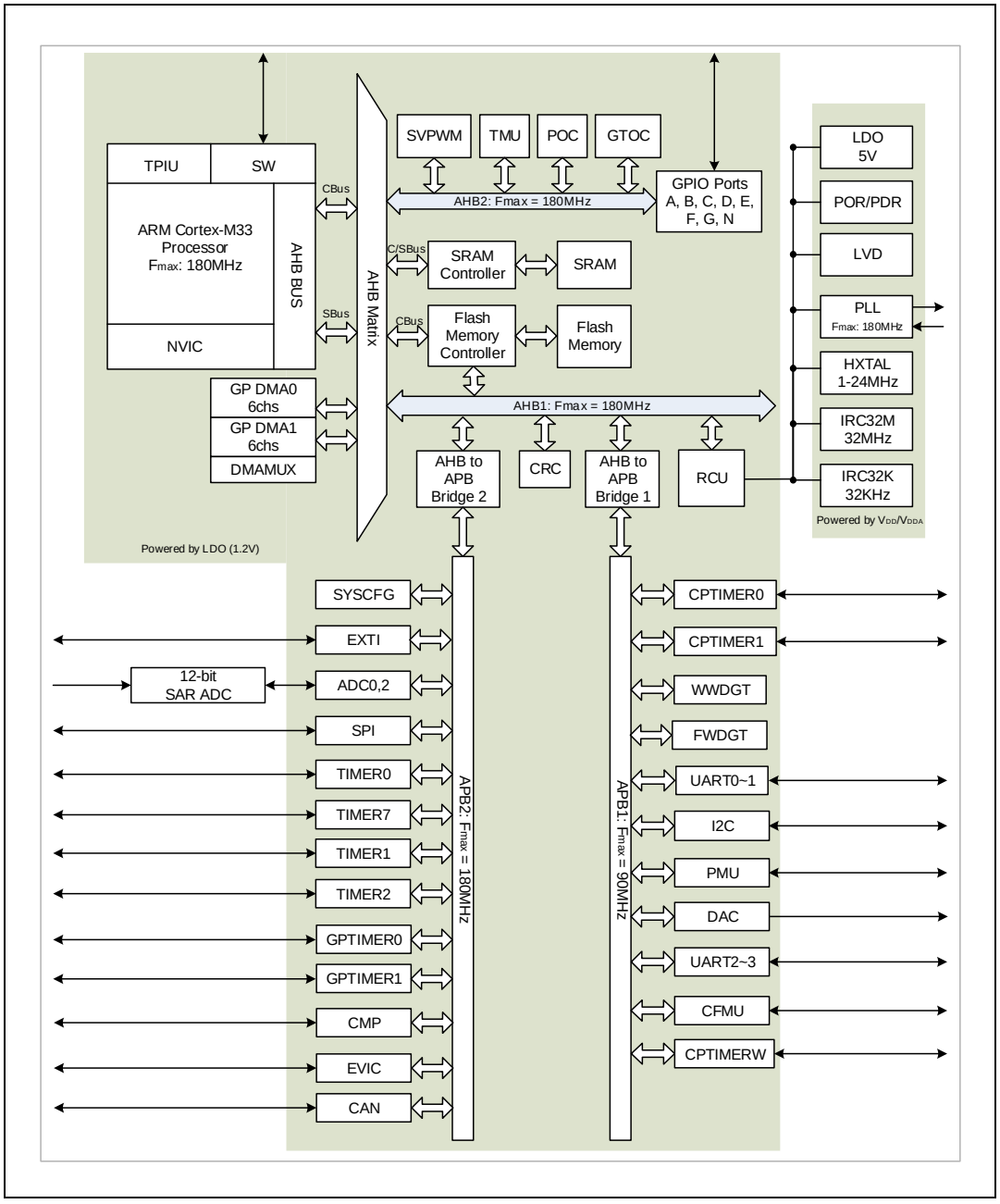
(2) General timer (GP TM) includes: GPTIMER0, GPTIMER1 (16bit x 2ch); TIMER1, TIMER2 (16bit x 4ch)

(3) Compare timer (CP TM) includes: CPTIMER0, CPTIMER1 (16bit x 2cnt); CPTIMERW (16bit/32bit x 2ch input, x 2ch output, x 2ch compare match)

(4) Tsensor is temperature sensor that are integrated within ADC2 and controlled uniformly by ADC2

2.2. Block diagram

Figure 2-1. GD32M531xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32M531Cx LQFP48 pinouts

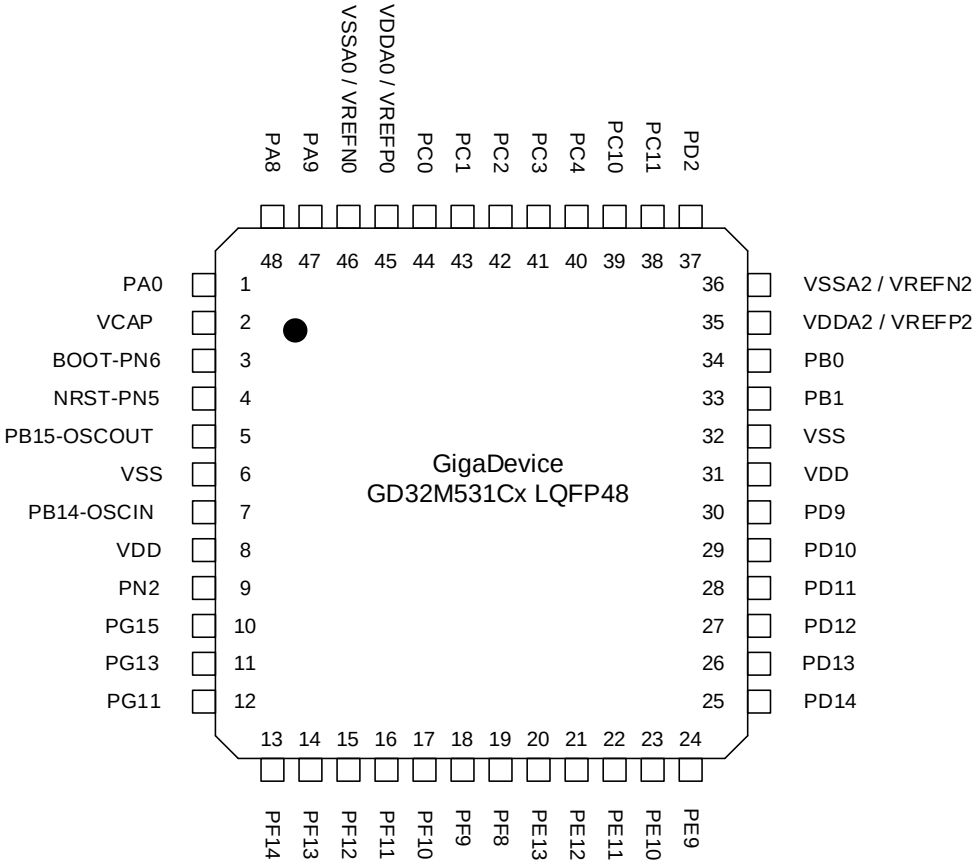
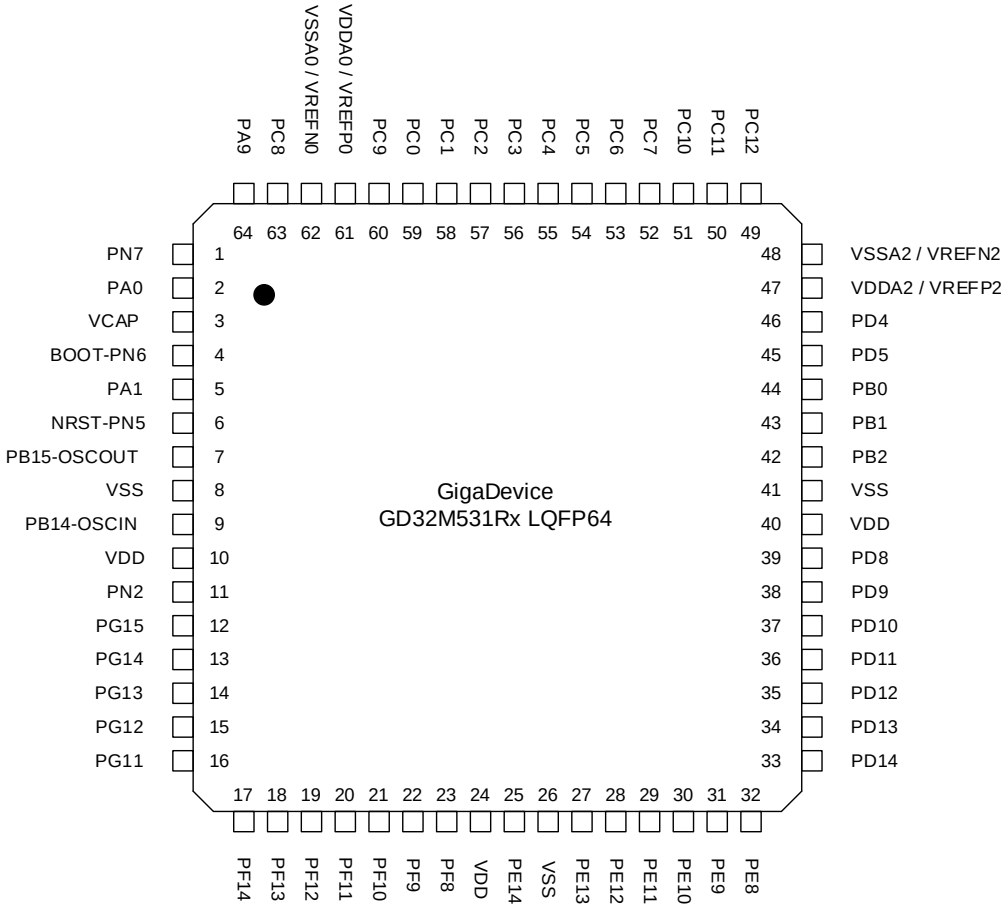


Figure 2-3. GD32M531Rx LQFP64 pinouts



2.4. Memory map

Table 2-2. GD32M531xx memory map

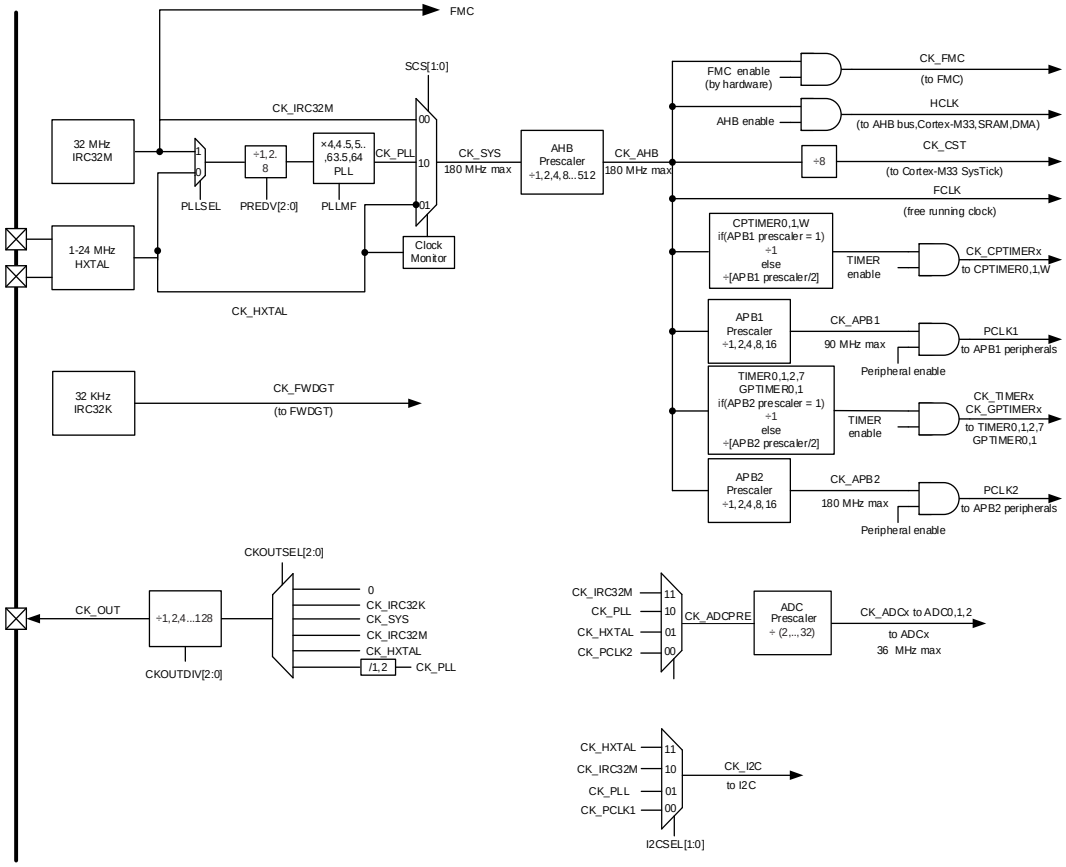
Pre-defined Regions	Bus	Address	Peripherals
External RAM		0x6000 0000 - 0xDFFF FFFF	Reserved
Peripheral		0x5000 0000 - 0x5FFF FFFF	Reserved
	AHB2	0x4802 4800 - 0x4FFF FFFF	Reserved
		0x4802 4400 - 0x4802 47FF	TMU
		0x4802 4000 - 0x4802 43FF	SVPWM
		0x4800 4C00 - 0x4802 3FFF	Reserved
		0x4800 4800 - 0x4800 4BFF	GTOC
		0x4800 4400 - 0x4800 47FF	POC
		0x4800 4000 - 0x4801 43FF	GPION
		0x4800 1C00 - 0x4800 3FFF	Reserved
		0x4800 1800 - 0x4800 1BFF	GPIOG
		0x4800 1400 - 0x4800 17FF	GPIOF

Pre-defined Regions	Bus	Address	Peripherals
		0x4800 1000 - 0x4800 13FF	GPIOE
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 3400 - 0x47FF FFFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0C00 - 0x4002 0FFF	Reserved
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
	APB2	0x4001 B000 - 0x4001 FFFF	Reserved
		0x4001 A000 - 0x4001 AFFF	CAN
		0x4001 8800 - 0x4001 9FFF	Reserved
		0x4001 8400 - 0x4001 87FF	EVIC
		0x4001 8000 - 0x4001 83FF	Reserved
		0x4001 7C00 - 0x4001 7FFF	CMP
		0x4001 6800 - 0x4001 7BFF	Reserved
		0x4001 6100 - 0x4001 67FF	GPTIMER1
		0x4001 6000 - 0x4001 60FF	GPTIMER0
		0x4001 4800 - 0x4001 5FFF	Reserved
		0x4001 4400 - 0x4001 47FF	TIMER2
		0x4001 4000 - 0x4001 43FF	TIMER1
		0x4001 3800 - 0x4001 7BFF	Reserved
		0x4001 3400 - 0x4001 37FF	TIMER7
		0x4001 3000 - 0x4001 33FF	SPI
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC2
		0x4001 2000 - 0x4001 23FF	ADC0
		0x4001 0800 - 0x4001 1FFF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI
		0x4001 0000 - 0x4001 03FF	SYSCFG
	APB1	0x4000 E400 - 0x4000 FFFF	Reserved
		0x4000 E000 - 0x4000 E3FF	CPTIMERW
		0x4000 CC00 - 0x4000 DFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CFMU

Pre-defined Regions	Bus	Address	Peripherals
		0x4000 8000 - 0x4000 C7FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	UART3
		0x4000 7800 - 0x4000 7BFF	UART2
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 5800 - 0x4000 6FFF	Reserved
		0x4000 5400 - 0x4000 57FF	I2C
		0x4000 5000 - 0x4000 53FF	UART1
		0x4000 4C00 - 0x4000 4FFF	UART0
		0x4000 3400 - 0x4000 4BFF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 1800 - 0x4000 2BFF	Reserved
		0x4000 0400 - 0x4000 07FF	CPTIMER1
		0x4000 0000 - 0x4000 03FF	CPTIMER0
SRAM		0x2000 8000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 7FFF	SRAM (32KB)
Code		0x1FFF F820 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF F81F	Option Bytes (32B)
		0x1FFF E000- 0x1FFF F7FF	System Memory (6KB)
		0x1FFF 7200 - 0x1FFF DFFF	Reserved
		0x1FFF 7000~0x1FFF 71FF	OTP (512B)
		0x1000 8000 - 0x1FFF 6FFF	Reserved
		0x1000 0000 - 0x1000 7FFF	SRAM Aliased
		0x0881 0000 - 0x0FFF FFFF	Reserved
		0x0880 0000 - 0x0880 FFFF	Data Flash (64KB)
		0x0804 0000 - 0x0807 FFFF	Reserved
		0x0800 0000 - 0x0803 FFFF	Main Flash (256KB)
		0x0002 6000 - 0x07FF FFFF	Reserved
		0x0000 0000 - 0x0002 5FFF	Aliased to Flash or system memory

2.5. Clock tree

Figure 2-4. GD32M531xx clock tree



Legend:

HXTAL: High speed crystal oscillator

IRC32M: Internal 32M RC oscillators

IRC32K: Internal 32K RC oscillator

2.6. Pin definitions

2.6.1. GD32M531Cx LQFP48 pin definitions

Table 2-3. GD32M531Cx LQFP48 pin definitions

GD32M531Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA9	47	I/O		Default: PA9 Alternate: TIMER0_CH3, TIMER_ETI3, TIMER0_CH3_INV, POC_IN3, UART3_RX, TIMER2_CH3, GPTIMER1_CH1, GTOC0_IN,

GD32M531Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				GPTIMER1_CH1_INV, GTOC2_IN, GPTIMER0_CPPO, EVENTOUT
PA8	48	I/O		Default: PA8 Alternate: TIMER2_CH1, TIMER_ETI4, POC_IN5, GPTIMER1_CH0, GTOC1_IN, GPTIMER1_CH0_INV, GTOC3_IN, EVENTOUT
PA0	1	I/O		Default: PA0 Alternate: CK_OUT, TIMER2_CH0, CFMUREF, UART3_RX, CMP0_OUT, EVENTOUT Additional: WKUP1
VCAP	2	P	-	Default: VCAP
BOOT-PN6	3	I/O		Default: BOOT, OL Alternate: EVENTOUT
NRST-PN5	4	I/O		Default: NRST Additional: PN5(3)
PB15-OSCOUT	5	I/O		Default: PB15 Alternate: UART1_RX, EVENTOUT Additional: OSCOUT
VSS	6	P	-	Default: VSS
PB14-OSCIN	7	I/O		Default: PB14 Alternate: UART1_TX, EVENTOUT Additional: OSCIN
VDD	8	P	-	Default: VDD
PN2	9	I/O		Default: SWCLK Alternate: POC_IN4, EVENTOUT Additional: NMI,SWCLK
PG15	10	I/O		Default: PG15 Alternate: TIMER2_CH0, UART1_TX, CAN_TX, SPI_NSS, GPTIMER0_CH0, GPTIMER1_CH0, GPTIMER0_CH0_INV, GPTIMER1_CH0_INV, EVENTOUT
PG13	11	I/O		Default: SWDIO Alternate: TIMER1_CH1, TIMER2_CH0, UART0_RX, GPTIMER0_CH0, GTOC0_IN, GPTIMER0_CH0_INV, EVENTOUT Additional: SWDIO
PG11	12	I/O		Default: PG11 Alternate: TIMER1_CH2, TIMER2_CH2, UART0_TX, GTOC2_IN, GPTIMER0_CH1, GPTIMER0_CH1_INV, EVENTOUT
PF14	13	I/O		Default: PF14

GD32M531Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: CPTIMERW_OC0, TIMER2_CH2, UART1_RX, UART3_RX, CAN_RX, GPTIMER1_CH0, GPTIMER1_CH0_INV, EVENTOUT
PF13	14	I/O		Default: PF13 Alternate: CPTIMERW_IC0, TIMER2_CH3, UART1_TX, UART3_TX, CAN_TX, GPTIMER1_CH1, GPTIMER1_CH1_INV, EVENTOUT
PF12	15	I/O		Default: PF12 Alternate: CK_OUT, POC_IN2, UART3_RX, CAN_RX, SPI_MISO, GTOC0_IN, GTOC1_IN, GTOC2_IN, GTOC3_IN, GPTIMER0_CPPO, EVENTOUT
PF11	16	I/O		Default: PF11 Alternate: CPTIMERW_OC1, TIMER1_CH0, CFMUREF, UART3_TX, CAN_TX, SPI_SCK, EVENTOUT
PF10	17	I/O	5VT	Default: PF10 Alternate: CPTIMERW_IC1, TIMER1_CH1, ADCSM1, UART2_TX, I2C_SMBA, I2C_SDA, SPI_IO3, ADCSM3, GPTIMER0_CH0, GPTIMER0_CH0_INV, EVENTOUT
PF9	18	I/O	5VT	Default: PF9 Alternate: TIMER1_CH2, ADCSM2, UART2_RX, I2C_SCL, SPI_IO2, ADCSM4, GPTIMER0_CH1, GPTIMER0_CH1_INV, EVENTOUT
PF8	19	I/O	5VT	Default: PF8 Alternate: TIMER1_CH3, ADC2_TRG, UART2_TX, I2C_SDA, I2C_SMBA, SPI_MOSI, GPTIMER0_CH0, GPTIMER0_CH0_INV, EVENTOUT
PE13	20	I/O		Default: PE13 Alternate: TIMER7_CH0, TIMER7_CH0_INV
PE12	21	I/O		Default: PE12 Alternate: TIMER7_CH1, TIMER7_CH1_INV
PE11	22	I/O		Default: PE11 Alternate: TIMER7_CH2, TIMER7_CH3, TIMER7_CH2_INV, TIMER7_CH3_INV
PE10	23	I/O		Default: PE10 Alternate: TIMER7_MCH0, TIMER7_MCH3, TIMER7_MCH0_INV, TIMER7_MCH3_INV
PE9	24	I/O		Default: PE9 Alternate: TIMER7_MCH1, TIMER7_MCH1_INV
PD14	25	I/O		Default: PD14 Alternate: TIMER0_MCH2, TIMER0_MCH2_INV
PD13	26	I/O		Default: PD13

GD32M531Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER0_MCH1, TIMER0_MCH1_INV
PD12	27	I/O		Default: PD12 Alternate: TIMER0_MCH0, TIMER0_MCH0_INV
PD11	28	I/O		Default: PD11 Alternate: TIMER0_CH2, TIMER0_CH2_INV
PD10	29	I/O		Default: PD10 Alternate: TIMER0_CH1, TIMER0_CH1_INV
PD9	30	I/O		Default: PD9 Alternate: TIMER0_CH0, TIMER0_CH0_INV
VDD	31	P	-	Default: VDD
VSS	32	P	-	Default: VSS
PB1	33	I/O		Default: PB1 Alternate: TIMER2_CH0, TIMER_ETI1, CMP3_OUT, UART3_TX, SPI_MOSI, EVENTOUT Additional: ADC2_IN7
PB0	34	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER_ETI2, ADC0_TRG, SPI_SCK, EVENTOUT Additional: ADC2_IN6
VDDA2 / VREFP2	35	P	-	Default: VDDA2
VSSA2 / VREFN2	36	P	-	Default: VSSA2
PD2	37	I/O		Default: PD2 Alternate: EVENTOUT Additional: ADC2_IN8,CMP3_INP2
PC11	38	I/O		Default: PC11 Alternate: EVENTOUT Additional: ADC2_IN1,CMP1_INP3,CMP_INN1
PC10	39	I/O		Default: PC10 Alternate: EVENTOUT Additional: ADC2_IN0,CMP0_INP3,CMP2_INP5
PC4	40	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC0_IN4,CMP0_INP2
PC3	41	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC0_IN3,CMP2_INP4,CMP3_INP1
PC2	42	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC0_IN2,CMP2_INP1
PC1	43	I/O		Default: PC1

GD32M531Cx LQFP48				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: EVENTOUT Additional: ADC0_IN1,CMP1_INP1
PC0	44	I/O		Default: PC0 Alternate: EVENTOUT Additional: ADC0_IN0,CMP0_INP1,CMP1_INP4
VDDA0 / VREFP0	45	P	-	Default: VDDA0
VSSA0 / VREFN0	46	P	-	Default: VSSA0

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the USER_1 bit field in the option byte of the GD32M531 User Manual to configure the NRST-PN5 pin as a PN5 general GPIO function.

2.6.2. GD32M531Rx LQFP64 pin definitions

Table 2-4. GD32M531Rx LQFP64 pin definitions

GD32M531Cx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PA9	64	I/O		Default: PA9 Alternate: TIMER0_CH3, TIMER_ETI3, TIMER0_CH3_INV, POC_IN3, UART3_RX, TIMER2_CH3, GPTIMER1_CH1, GTOC0_IN, GPTIMER1_CH1_INV, GTOC2_IN, GPTIMER0_CPPO, EVENTOUT
PN7	1	I/O		Default: TSEL Alternate: TIMER2_CH3, ADC0_PROC, EVENTOUT Additional: TSEL
PA0	2	I/O		Default: PA0 Alternate: CK_OUT, TIMER2_CH0, CFMUREF, UART3_RX, CMP0_OUT, EVENTOUT Additional: WKUP1
VCAP	3	P	-	Default: VCAP
BOOT-PN6	4	I/O		Default: BOOT, OL Alternate: EVENTOUT
PA1	5	I/O		Default: PA1 Alternate: TIMER2_CH2, POC_IN5, ADC2_PROC, UART3_TX, CMP1_OUT, GTOC0_IN, GTOC1_IN, GTOC2_IN, GTOC3_IN, EVENTOUT

GD32M531Cx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
NRST-PN5	6	I/O		Default: NRST Additional: PN5(3)
PB15-OSCOUT	7	I/O		Default: PB15 Alternate: UART1_RX, EVENTOUT Additional: OSCOUT
VSS	8	P	-	Default: VSS
PB14-OSCIN	9	I/O		Default: PB14 Alternate: UART1_TX, EVENTOUT Additional: OSCIN
VDD	10	P	-	Default: VDD
PN2	11	I/O		Default: PN2 Alternate: POC_IN4, EVENTOUT Additional: NMI
PG15	12	I/O		Default: PG15 Alternate: TIMER2_CH0, UART1_TX, CAN_TX, SPI_NSS, GPTIMER0_CH0, GPTIMER1_CH0, GPTIMER0_CH0_INV, GPTIMER1_CH0_INV, EVENTOUT Additional: NJTRST
PG14	13	I/O		Default: PG14 Alternate: TIMER2_CH2, ADC0_PROC, UART3_RX, SPI_NSS, GPTIMER0_CH1, GPTIMER1_CH1, GPTIMER0_CH1_INV, GPTIMER1_CH1_INV, EVENTOUT Additional: JTMS, SWDIO
PG13	14	I/O		Default: JTDI Alternate: TIMER1_CH1, TIMER2_CH0, UART0_RX, GPTIMER0_CH0, GTOC0_IN, GPTIMER0_CH0_INV, EVENTOUT Additional: JTDI
PG12	15	I/O		Default: PG12 Alternate: TIMER2_CH1, UART3_TX, GPTIMER0_CH1, GTOC1_IN, GPTIMER0_CH1_INV, EVENTOUT Additional: JTCK, SWCLK
PG11	16	I/O		Default: PG11 Alternate: TIMER1_CH2, TIMER2_CH2, UART0_TX, GTOC2_IN, GPTIMER0_CH1, GPTIMER0_CH1_INV, EVENTOUT Additional: JTDO, TRACESWO
PF14	17	I/O		Default: PF14

GD32M531Cx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: CPTIMERW_OC0, TIMER2_CH2, UART1_RX, UART3_RX, CAN_RX, GPTIMER1_CH0, GPTIMER1_CH0_INV, EVENTOUT
PF13	18	I/O		Default: PF13 Alternate: CPTIMERW_IC0, TIMER2_CH3, UART1_TX, UART3_TX, CAN_TX, GPTIMER1_CH1, GPTIMER1_CH1_INV, EVENTOUT
PF12	19	I/O		Default: PF12 Alternate: CK_OUT, POC_IN2, UART3_RX, CAN_RX, SPI_MISO, GTOC0_IN, GTOC1_IN, GTOC2_IN, GTOC3_IN, GPTIMER0_CPPO, EVENTOUT
PF11	20	I/O		Default: PF11 Alternate: CPTIMERW_OC1, TIMER1_CH0, CFMUREF, UART3_TX, CAN_TX, SPI_SCK, EVENTOUT
PF10	21	I/O	5VT	Default: PF10 Alternate: CPTIMERW_IC1, TIMER1_CH1, ADCSM1, UART2_TX, I2C_SMBA, I2C_SDA, SPI_IO3, ADCSM3, GPTIMER0_CH0, GPTIMER0_CH0_INV, EVENTOUT
PF9	22	I/O	5VT	Default: PF9 Alternate: TIMER1_CH2, ADCSM2, UART2_RX, I2C_SCL, SPI_IO2, ADCSM4, GPTIMER0_CH1, GPTIMER0_CH1_INV, EVENTOUT
PF8	23	I/O	5VT	Default: PF8 Alternate: TIMER1_CH3, ADC2_TRG, UART2_TX, I2C_SDA, I2C_SMBA, SPI_MOSI, GPTIMER0_CH0, GPTIMER0_CH0_INV, EVENTOUT
VDD	24	P	-	Default: VDD
PE14	25	I/O		Default: PE14 Alternate: POC_IN1, TIMER7_BRKIN, GTOC0_IN, GTOC1_IN, GTOC2_IN, GTOC3_IN, GPTIMER1_CPPO, EVENTOUT
VSS	26	P	-	Default: VSS
PE13	27	I/O		Default: PE13 Alternate: TIMER7_CH0, TIMER7_CH0_INV
PE12	28	I/O		Default: PE12 Alternate: TIMER7_CH1, TIMER7_CH1_INV
PE11	29	I/O		Default: PE11 Alternate: TIMER7_CH2, TIMER7_CH3,

GD32M531Cx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				TIMER7_CH2_INV, TIMER7_CH3_INV
PE10	30	I/O		Default: PE10 Alternate: TIMER7_MCH0, TIMER7_MCH3, TIMER7_MCH0_INV, TIMER7_MCH3_INV
PE9	31	I/O		Default: PE9 Alternate: TIMER7_MCH1, TIMER7_MCH1_INV
PE8	32	I/O		Default: PE8 Alternate: TIMER7_MCH2, TIMER7_MCH2_INV
PD14	33	I/O		Default: PD14 Alternate: TIMER0_MCH2, TIMER0_MCH2_INV
PD13	34	I/O		Default: PD13 Alternate: TIMER0_MCH1, TIMER0_MCH1_INV
PD12	35	I/O		Default: PD12 Alternate: TIMER0_MCH0, TIMER0_MCH0_INV
PD11	36	I/O		Default: PD11 Alternate: TIMER0_CH2, TIMER0_CH2_INV
PD10	37	I/O		Default: PD10 Alternate: TIMER0_CH1, TIMER0_CH1_INV
PD9	38	I/O		Default: PD9 Alternate: TIMER0_CH0, TIMER0_CH0_INV
PD8	39	I/O		Default: PD8 Alternate: TIMER1_CH0, TIMER_ETI3, POC_IN0, TIMER0_BRKIN, SPI_NSS, GTOC0_IN, GTOC1_IN, GTOC2_IN, GTOC3_IN, GPTIMER0_CPPO, EVENTOUT
VDD	40	P	-	Default: VDD
VSS	41	P	-	Default: VSS
PB2	42	I/O		Default: PB2 Alternate: TIMER1_CH2, TIMER_ETI4, ADC2_TRG, CMP2_OUT, TIMER2_CH1, UART3_RX, SPI_MISO, CAN_RX, EVENTOUT
PB1	43	I/O		Default: PB1 Alternate: TIMER2_CH0, TIMER_ETI1, CMP3_OUT, UART3_TX, SPI_MOSI, EVENTOUT Additional: ADC2_IN7
PB0	44	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER_ETI2, ADC0_TRG, SPI_SCK, EVENTOUT Additional: ADC2_IN6
PD5	45	I/O		Default: PD5 Alternate: EVENTOUT

GD32M531Cx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC2_IN5, CMP3_INP4, DAC0_OUT1
PD4	46	I/O		Default: PD4 Alternate: EVENTOUT Additional: ADC2_IN4, CMP3_INP3, DAC0_OUT0
VDDA2/VREFP2	47	P	-	Default: VDDA2
VSSA2/VREFN2	48	P	-	Default: VSSA2
PC12	49	I/O		Default: PC12 Alternate: EVENTOUT Additional: ADC2_IN2, CMP2_INP3,CMP_INN2
PC11	50	I/O		Default: PC11 Alternate: EVENTOUT Additional: ADC2_IN1, CMP1_INP3,CMP_INN1
PC10	51	I/O		Default: PC10 Alternate: EVENTOUT Additional: ADC2_IN0, CMP0_INP3,CMP2_INP5
PC7	52	I/O		Default: PC7 Alternate: EVENTOUT Additional: ADC2_IN3, CMP0_INP4
PC6	53	I/O		Default: PC6 Alternate: EVENTOUT Additional: ADC0_IN6, CMP2_INP2
PC5	54	I/O		Default: PC5 Alternate: EVENTOUT Additional: ADC0_IN5, CMP1_INP2
PC4	55	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC0_IN4, CMP0_INP2
PC3	56	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC0_IN3, CMP2_INP4 , CMP3_INP1
PC2	57	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC0_IN2, CMP2_INP1
PC1	58	I/O		Default: PC1 Alternate: EVENTOUT Additional: ADC0_IN1, CMP1_INP1
PC0	59	I/O		Default: PC0 Alternate: EVENTOUT

GD32M531Cx LQFP64				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Additional: ADC0_IN0, CMP0_INP1, CMP1_INP4
PC9	60	I/O		Default: PC9 Alternate: UART3_RX Additional: ADC2_IN9, CMP3_INP5
VDDA0/VREFP0	61	P	-	Default: VDDA0
VSSA0/VREFN0	62	P	-	Default: VSSA0
PC8	63	I/O		Default: PC8 Alternate: TIMER0_MCH3, TIMER2_CH1, TIMER0_MCH3_INV, UART3_TX, GPTIMER1_CH0, GPTIMER1_CH0_INV

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Refer to the description of the USER_1 bit field in the option byte of the GD32M531 User Manual to configure the NRST-PN5 pin as a PN5 general GPIO function

2.6.3. GD32M531xx pin alternate functions

Table 2-5. Port A alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	CK_OUT	TIMER2_CH0				CFMUREF	UART3_RX		CMP0_OUT							EVENTOUT
PA1		TIMER2_CH2			POC_IN5	ADC0_PROC	UART3_TX		CMP1_OUT		GTOC0_IN	GTOC1_IN	GTOC2_IN	GTOC3_IN		EVENTOUT
PA8		TIMER2_CH1	TIMER_ETI4				POC_IN5				GPTIMER1_CH0	GTOC1_IN	GPTIMER1_CH0_INV	GTOC3_IN		EVENTOUT
PA9		TIMER0_CH3	TIMER_ETI3	TIMER0_CH3_INV			POC_IN3	UART3_RX		TIMER2_CH3	GPTIMER1_CH1	GTOC0_IN	GPTIMER1_CH1_INV	GTOC2_IN	GPTIMER0_CPPO	EVENTOUT

Table 2-6. Port B alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER2_CH2	TIMER_ETI2					ADC0_TRG				SPI_SCK				EVENTOUT
PB1		TIMER2_CH0	TIMER_ETI1						CMP3_OUT		UART3_TX	SPI_MOSI				EVENTOUT
PB2		TIMER1_CH2	TIMER_ETI4					ADC2_TRG	CMP2_OUT	TIMER2_CH1	UART3_RX	SPI_MISO		CAN_RX		EVENTOUT
OSCIN-PB14							UART1_TX									EVENTOUT
OSCOUT-PB15							UART1_RX									EVENTOUT

Table 2-7. Port C alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0																EVENT OUT
PC1																EVENT OUT
PC2																EVENT OUT
PC3																EVENT OUT
PC4																EVENT OUT
PC5																EVENT OUT
PC6																EVENT OUT
PC7																EVENT OUT
PC9								UART3_RX								
PC8			TIMER0_MCH3	TIMER2_CH1	TIMER0_MCH3_INV			UART3_TX				GPTIMER1_CH0		GPTIMER1_CH0_INV		
PC10																EVENT OUT
PC11																EVENT OUT
PC12																EVENT OUT

Table 2-8. Port D alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD2																EVENT OUT
PD4																EVENT OUT
PD5																EVENT OUT
PD8		TIMER1	TIMER_				POC_IN	TIMER0		SPI_NS	GTOC0_	GTOC1_	GTOC2_	GTOC3_	GPTIME	EVENT

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		_CH0	ETI3				0	_BRKIN		S	IN	IN	IN	IN	R0_CPPO	OUT
PD9		TIMER0_CH0		TIMER0_CH0_INV												
PD10		TIMER0_CH1		TIMER0_CH1_INV												
PD11		TIMER0_CH2		TIMER0_CH2_INV												
PD12		TIMER0_MCH0		TIMER0_MCH0_INV												
PD13		TIMER0_MCH1		TIMER0_MCH1_INV												
PD14		TIMER0_MCH2		TIMER0_MCH2_INV												

Table 2-9. Port E alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE8		TIMER7_MCH2		TIMER7_MCH2_INV												
PE9		TIMER7_MCH1		TIMER7_MCH1_INV												
PE10		TIMER7_MCH0	TIMER7_MCH3	TIMER7_MCH0_INV	TIMER7_MCH3_INV											
PE11		TIMER7_CH2	TIMER7_CH3	TIMER7_CH2_INV	TIMER7_CH3_INV											
PE12		TIMER7_CH1		TIMER7_CH1_I												

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
				NV												
PE13		TIMER7_CH0		TIMER7_CH0_INV												
PE14							POC_IN1	TIMER7_BRKIN			GTOC0_IN	GTOC1_IN	GTOC2_IN	GTOC3_IN	GPTIMER1_CPPO	EVENTOUT

Table 2-10. Port F alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF8		TIMER1_CH3				ADC2_TRG	UART2_TX	I2C_SDA	I2C_SMBA	SPI_MOSI		GPTIMER0_CH0		GPTIMER0_CH0_INV		EVENTOUT
PF9		TIMER1_CH2				ADCSM2	UART2_RX		I2C_SCL	SPI_IO2	ADCSM4	GPTIMER0_CH1		GPTIMER0_CH1_INV		EVENTOUT
PF10	CPTIMERW_IC1	TIMER1_CH1				ADCSM1	UART2_TX	I2C_SMBA	I2C_SDA	SPI_IO3	ADCSM3	GPTIMER0_CH0		GPTIMER0_CH0_INV		EVENTOUT
PF11	CPTIMERW_OC1	TIMER1_CH0				CFMUREF		UART3_TX	CAN_TX	SPI_SCK						EVENTOUT
PF12	CK_OUT				POC_IN2			UART3_RX	CAN_RX	SPI_MISO	GTOC0_IN	GTOC1_IN	GTOC2_IN	GTOC3_IN	GPTIMER0_CPPO	EVENTOUT
PF13	CPTIMERW_IC0			TIMER2_CH3			UART1_TX	UART3_TX	CAN_TX			GPTIMER1_CH1		GPTIMER1_CH1_INV		EVENTOUT
PF14	CPTIMERW_OC0	TIMER2_CH2					UART1_RX	UART3_RX	CAN_RX			GPTIMER1_CH0		GPTIMER1_CH0_INV		EVENTOUT

Table 2-11. Port G alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG11		TIMER1_CH2		TIMER2_CH2			UART0_TX					GTOC2_IN		GPTIMER0_CH1	GPTIMER0_CH1_INV	EVENTOUT

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG12				TIMER2_CH1				UART3_TX			GPTIMER0_CH1	GTOC1_IN	GPTIMER0_CH1_INV			EVENTOUT
PG13		TIMER1_CH1		TIMER2_CH0			UART0_RX				GPTIMER0_CH0	GTOC0_IN	GPTIMER0_CH0_INV			EVENTOUT
PG14		TIMER2_CH2				ADC0_PROC		UART3_RX		SPI_NSS	GPTIMER0_CH1	GPTIMER1_CH1	GPTIMER0_CH1_INV	GPTIMER1_CH1_INV		EVENTOUT
PG15		TIMER2_CH0					UART1_TX		CAN_TX	SPI_NSS	GPTIMER0_CH0	GPTIMER1_CH0	GPTIMER0_CH0_INV	GPTIMER1_CH0_INV		EVENTOUT

Table 2-12. Port N alternate functions summary

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PN2							POC_IN4									EVENTOUT
NRST-PN5																
BOOT-PN6																EVENTOUT
PN7		TIMER2_CH3				ADC0_PROC										EVENTOUT

3. Functional description

3.1. Arm® Cortex®-M33 core

The Cortex®-M33 processor is a 32-bit processor that possesses low interrupt latency and low-cost debug. The characteristics of integrated and advanced make the Cortex®-M33 processor suitable for market products that require microcontrollers with high performance and low power consumption. The Cortex®-M33 processor is based on the Armv8 architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations and DSP. Some system peripherals listed below are also provided by Cortex®-M33:

- Internal Bus Matrix connected with Code bus, System bus, and Private Peripheral Bus (PPB) and debug accesses.
- Nested Vectored Interrupt Controller (NVIC).
- Breakpoint Unit (BPU).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Serial Wire JTAG Debug Port (SWJ-DP).
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU)
- Floating Point Unit (FPU).
- DSP Extension (DSP).
- Support External coprocessor for TMU.

3.2. Embedded memory

- Up to 32KB of on-chip SRAM
- Up to 256KB of main flash memory.
- Up to 64KB of data flash memory.
- Up to 512B OTP (One Time Programmable) memory for user data storage.
- Up to 6KB of information blocks for the bootloader.
- 32B Option bytes to configure the device.
- ECC with single bit error corrected and double bit errors detected.

Up to 320 Kbytes of inner Flash memory, and up to 64 Kbytes of inner SRAM at most is available for storing programs and data, and Flash is accessed (read) at CPU clock speed with 0~6 wait states.***Table 2-2. GD32M531xx memory map*** shows the memory map of the GD32M531xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- 1 to 24 MHz High speed crystal oscillator (HXTAL)
- Internal 32 MHz RC oscillator (IRC32M)
- Internal 32 KHz RC oscillator (IRC32K)
- PLL clock source can be HXTAL or IRC32M
- HXTAL clock monitor
- Two power domains: V_{DD} / V_{DDA} domain and V_{CORE} domain.
- Three power saving modes: Sleep, Deep-sleep and Standby modes.
- Internal Voltage regulator (LDO) supplies 1.2V voltage source for V_{CORE} domain.
- Three Low Voltage Detectors (LVD) to detect low voltage events. LVD1 / LVD2 can generate interrupts. LVD0 / LVD1 / LVD2 can generate a system reset.

The clock control unit provides a range of frequencies and clock functions. These include an Internal 32 MHz RC oscillator (IRC32M), a high speed crystal oscillator (HXTAL), an Internal 32KHz RC oscillator (IRC32K), a Phase Lock Loop (PLL), a HXTAL clock monitor, PLL Clock Monitor (PLLM), clock prescalers, clock multiplexers and clock gating circuitry. The frequency of AHB, APB2 and the APB1 domains can be configured by each prescaler. The maximum frequency of the AHB, APB2 and APB1 domains is 180 MHz/180 MHz/90 MHz.See ***Figure 2-4. GD32M531xx clock tree*** for details on the clock tree.

The reset control unit includes the control of 2 kinds of reset: power reset, system reset. The power on reset, known as a cold reset, resets the full system except the backup domain during a power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller and the backup domain. The resets can be triggered by an external signal, internal events and the reset generators.

Power supply schemes:

- V_{DD} range: 2.7V to 5.5V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins
- V_{SSA0}, V_{DDA0} range: 2.7V to 5.5V, external analog power supplies for ADC0 V_{DDA0} and V_{SSA0} must be connected to V_{DDA0} and V_{SSA0}, respectively
- V_{SSA2}, V_{DDA2} range: 2.7V to 5.5V, external analog power supplies for ADC2, DAC0 and CMPs. V_{DDA2} and V_{SSA2} must be connected to V_{DDA2} and V_{SSA2}, respectively.

3.4. Boot modes

At startup, boot pins are used to select one of four boot options:

- Boot from main Flash memory (default)
- Boot from system memory

GD32M531xx devices provide two kinds of boot sources which can be selected by the BOOT-PN6. The details are shown in the following table. The value on the two pins is latched on the 4th rising edge of CK_SYS after a reset. It is up to the user to set the BOOT-PN6 pin after a

power-on reset or a system reset to select the required boot source. Once the pin have been sampled, they are free and can be used for other purposes.

Table 3-1. Boot modes

Selected boot source	Boot mode selection pin
	BOOT-PN6
System Memory	0
Main Flash Memory	1

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory by using UART2(PF10 and PF9), UART3(PF13 and PF14), or UART3(PF11 and PF12). It also can be used to transfer and update the Flash memory code; the data and the vector table sections.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.
- **Deep-sleep mode**
  In deep-sleep mode, all clocks in the V_{CORE} domain are off, and all of the high speed crystal oscillator (IRC32M, HXTAL) and PLLs are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode. When exiting the deep-sleep mode, the IRC32M is selected as the system clock.
- **Standby mode**
  In standby mode, the whole V_{CORE} domain is power off, the LDO is shut down, and all of IRC32M, HXTAL and PLL are disabled. The contents of SRAM and registers in V_{CORE} power domain (except backup registers) are lost. There are three wakeup sources for the standby mode, including the external reset from NRST pin, the FWDGT reset and the rising edge on WKUP pin.

3.6. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Each pin weak pull-up / pull-down function.
- Output push-pull/open drain enable control
- Analog input/output configuration
- Alternate function input/output configuration

- External interrupt with programmable trigger edge – using EXTI configuration registers.

There are up to 53 general purpose I/O pins (GPIO), named PA0~PA1, PA9, PB0 ~ PB2, PB14 ~ PB15, PC0 ~ PC12, PD4 ~ PD14, PE8 ~ PE14, PF8 ~ PF14, PG11, PG13, PG15, PN2, PN5, PN6, PN7 for the devices GD32M531Rx, and up to 39 general purpose I/O pins (GPIO), named PA0, PA8 ~ PA9, PB0 ~ PB2, PB14 ~ PB15, PC0 ~ PC7, PC8, PC9, PC10 ~ PC12, PD2, PD4 ~ PD5, PD8 ~ PD14, PE8 ~ PE14, PF8 ~ PF14, PG11 ~ PG15, PN2, PN5, PN6 for the devices GD32M531Cx, to implement logic input / output functions.Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt / Event Controller Unit (EXTI).

The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Each GPIO pin can be configured as pull-up, pull-down or no pull-up / pull-down. All GPIOs are high-current capable except for analog mode.

3.7. Clock frequency measurement unit (CFMU)

- Clock frequency measurement for different target clocks: HXTAL, IRC32M, IRC32K or PCLK1.
- Selectable reference clocks: external clock input to CFMUREF pin, HXTAL, IRC32M, IRC32K or PCLK1.
- Digital filter function on CFMUREF pin.
- Interrupts and flags to indicate the clock frequency measurement status: clock measurement end, clock frequency error or overflow.

The clock frequency measurement unit provides a clock frequency accuracy measurement function. Count the pulses of the measured clock using the reference clock as the time base, and then determine whether the accuracy of the clock to be measured is within an allowable range through the count result. An interrupt request will be generated when the clock frequency accuracy measurement is completed or the count number of pulses is not within the allowable range.

3.8. Port Output Controller (POC)

- POC_INn (n=0,1…5) pin input detection:
  - Edge detection.
  - Level detection.
  - Configurable sampling clock frequency.

  - Optional valid sampling times.
  - Input inverting control.
- Request sources for pin disable:
  - From POC_INn (n=0,1…5) pin input detection.
  - From TIMER0/7 complementary PWM channel output detection.
  - From software generation.
  - From HXTAL stuck event.
  - From CPU LOCKUP event.
  - From comparator output detection.
- Selectable target TIMER for pin disable.
- Detection masking function:
  - Mask POC_INn (n=0,1…5) pin input detection.
  - Mask comparator output detection.
- Interrupt generation:
  - Valid signal input of POC_INn (n=0,1…5) pin.
  - Concurrent active-level outputs of TIMER0/7 complementary PWM channels.

The POC (Port Output Controller) can be used to disable pin outputs from the TIMER and GPTIMER channels in a variety of situations. The disabled output pins can choose high-impedance state (Hi-Z) output or general purpose I/O (GPIO) control output. These pins can be disabled by the POC module only if they select the TIMER or GPTIMER channels output as alternate function.

3.9. GPTIMER Output Controller (GTOC)

- GTOCx_IN (x=0…3) pin input detection:
  - Edge detection.
  - Level detection.
  - Input inverting control.
  - Digital filter
- Request sources for GPTIMER output close:
  - GTOCx_IN (x=0…3) pin input detection.
  - GPTIMER output fault detection (concurrent low or high level output on channel 0 and channel 1)
  - Software request generation.
  - HXTAL stuck event.
  - CPU LOCKUP event.
  - Comparator output detection.
- Request masking function:
  - Output closing request can be masked by GPTIMER output signals.
  - Extended closing request can be masked by GPTIMER output signals.
- Interrupt generation:
  - Valid signal input of GTOCx_IN (x=0…3) pin.

- GPTIMER output fault or comparator valid edge output.

The GTOC can generate request to close the output pin of GPTIMER. The closed pins can output Hi-Z state. Output closing request sources can come from different modules on the chip, such as CMP, GPTIMER and so on.

3.10. CRC calculation unit (CRC)

- Supports 7 / 8 / 16 / 32bits data input.
- For 7(8) / 16 / 32 bit input data length, the calculation cycles are 1 / 2 / 4 AHB clock cycles.
- For 32-bit input data length, the calculation cycle can be 1 AHB clock cycle (32-bit parallel CRC calculation with two fixed polynomials).
- User configurable polynomial value and size.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy checks management (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data.

This CRC management unit can be used to calculate 7 / 8 / 16 / 32 bit CRC code within user configurable polynomials.

3.11. Trigonometric Math Unit (TMU)

- 5 kinds of functions.
- The fixed point q1.31 / q1.15 format or IEEE754 32-bit single precision floating-point format is configurable.
- Programmable precision.
- CORDIC-algorithm core: circular system and hyperbolic system, rotation pattern and vectoring pattern.
- As an external coprocessor for CPU.

The Trigonometric Math Unit (TMU) is a fully configurable block that execute common trigonometric and arithmetic operations. The TMU can reduce the burden of CPU, and it is usually used in motor control, signal processing and many other applications.

3.12. Direct memory access controller (DMA)

- Programmable length of data to be transferred, max to 65536.
- 12 channels (6 for DMA0 and 6 for DMA1) and each channel are configurable.
- AHB and APB peripherals, FLASH, SRAM can be accessed as source and destination.
- Each channel is connected to fixed hardware DMA request.
- Software DMA channel priority (low, medium, high, ultra high) and hardware DMA

channel priority (DMA channel 0 has the highest priority and DMA channel 5 has the lowest priority).

- Support independent 8, 16, 32-bit memory and peripheral transfer.
- Support independent fixed and increasing address generation algorithm of memory and peripheral.
- Support circular transfer mode.
- Support peripheral to memory, memory to peripheral, and memory to memory transfers.
- One separate interrupt per channel with three types of event flags.
- Support interrupt enable and clear.

The direct memory access (DMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Data can be quickly moved by DMA between peripherals and memory as well as memory and memory without any CPU actions. There are 12 channels in the DMA controller (6 for DMA0 and 6 for DMA1). Each channel is dedicated to manage memory access requests from one or more peripherals. An arbiter is implemented inside to handle the priority among DMA requests.

The system bus is shared by the DMA controller and the Cortex®-M33 core. When the DMA and the CPU are targeting the same destination, the DMA access may stop the CPU access to the system bus for some bus cycles. Round-robin scheduling is implemented in the bus matrix to ensure at least half of the system bus bandwidth for the CPU.

3.13. DMA request multiplexer (DMAMUX)

- 12 channels for DMAMUX request multiplexer.
- 4 channels for DMAMUX request generator.
- Support 27 trigger inputs.
- Support 27 synchronization inputs.
- Each DMAMUX request generator channel:
  - DMA request trigger input selector
  - DMAMUX request generator counter
  - Trigger overrun flag
- Each DMAMUX request multiplexer channel:
  - 84 input DMA request lines from peripherals
  - Synchronization input selector
  - One DMA request line output
  - One channel event output, for DMA request chaining
  - DMAMUX request multiplexer counter
  - Synchronization overrun flag

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer

channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.14. Debug (DBG)

The GD32M531xx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the ARM® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the ARM® Cortex®-M33. The debug system supports serial wire debug (SWD), trace functions and standard JTAG debug. The debug and trace functions refer to the Cortex®-M33 Technical Reference Manual.

The DBG hold unit helps debugger to debug in power saving mode. When corresponding bit is set, it provides a clock in power saving mode or holds the state for TIMER, I2C, WWDGT, FWDGT or CAN.

3.15. Analog to digital converter (ADC)

- High performance.
  - ADC programmable sampling resolution: 12-bit, 10-bit, 8-bit or 6-bit.
  - Programmable A/D sampling time.
  - Programmable Sample and Hold time for sample-and-hold circuit.
  - Programmable disconnection-detection time (precharge and discharge).
  - Data storage mode: the most significant bit (MSB) alignment and the least significant bit (LSB) alignment.
  - DMA support.
- Analog function.
  - 7 external analog inputs for ADC0.
  - 10 external analog inputs channel, an internal reference voltage channel and an internal temperature sensor channel for ADC2.
  - Channel-dedicated sample-and-hold function (three channels for ADC0 only).
  - Analog input disconnection detection assist function (discharge function/precharge function)
- Start-of-conversion can be initiated.
  - Software trigger.
  - Synchronous trigger (from timer).
  - Asynchronous trigger. A/D conversion can be triggered by the external trigger ADC0_TRG pin (for ADC0), ADC2_TRG pin (for ADC2) (independently for two units).
- Operating modes
  - Group_pri1 scan once mode: A/D conversion is performed only once on the

selected channel in Group_pri1.

- Group_pri1 scan continuous mode: A/D conversion is performed repeatedly on the selected channel in Group_pri1.
- Groups scan mode (group priority control can be enabled or disabled): two groups (Group_pri1 & Group_pri2), three groups (Group_pri1 & Group_pri2 & Group_pri3 or Group_pri1 & Group_pri2 & Group_pri4) or four groups (Group_pri1 & Group_pri2 & Group_pri3 & Group_pri4). A/D conversion is performed only once on the selected channel in every group.

- Conversion result threshold monitor function: analog watchdog A and B.
- Bifurcate trigger mode: The conversion results of the same channel are stored in different data registers.
- Interrupt generation.
  - End of conversion round flag of Group_pri1/Group_pri2/Group_pri3/Group_pri4.
  - The watchdog event (watchdog A channel x compare status or watchdog B compare flag)
  - DMA overflow event of Group_pri1/Group_pri2/Group_pri3/Group_pri4.
- Oversampler: selectable A/D-converted value addition mode or average mode.
  - 32-bit data register.
  - Addition count select from 1,2,3,4,16,32,64-time.
- Channel dedicated data register.
- Channel input range: $V_{REFN} \leq V_{IN} \leq V_{REFP}$.

Two 12-bit successive approximation analog-to-digital converter module (ADC0/2) are integrated on the MCU chip and work independently.

ADC0 can sample 7 external channels, and ADC2 can sample 10 external channels and 2 internal channels (V_{REFINT}, V_{SENSE}). These selected sampling channels in each ADC module all support a variety of scan modes: Group_pri1 scan once mode, Group_pri1 scan continuous mode, or Groups scan mode. After each channel sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit (LSB) alignment or the most significant bit (MSB) alignment.

In Group_pri1 mode scan once mode, the selected external channels are converted in ascending channel order with the default channel priority. In Group_pri1 scan continuous mode, the selected external channels are converted in ascending channel order continuously with the default channel priority. In Groups mode scan mode, the selected external channels can be arbitrarily divided into two groups (Group_pri1 & Group_pri2), three groups (Group_pri1 & Group_pri2 & Group_pri3 or Group_pri1 & Group_pri2 & Group_pri4) or four groups (Group_pri1 & Group_pri2 & Group_pri3 & Group_pri4). The channels in each group are converted once in ascending channel order with the default channel priority when the trigger for the corresponding group is acknowledged.

The channel priority is configureable, and the group priority is fixed (Group_pri1 > Group_pri2 > Group_pri3 > Group_pri4). During the channel conversion of low-priority group, the trigger from the high-priority group will be acknowledged, and the ADC aborts the current conversion and starts the channel conversion of high-priority group. After the high-priority group is done,

the low-priority group conversion can be resumed from the last aborted channel or the scan start channel. Alternatively, the ADC has the option to skip the conversion of the low-priority group.

In bifurcate trigger mode, only one channel can be selected in each single scan group. The conversion results of the first trigger signal and the second trigger signal will be stored in different data registers.

When the self-diagnosis function is enabled, it is executed once at the beginning of each scan, converting one of the three internally generated diagnostic voltages.

An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

3.16. Digital to analog converter (DAC)

- 12-bit resolution.
- Left or right data alignment.
- Conversion update synchronously.
- Conversion triggered by external triggers.
- Extern voltage reference, V_{REFP}.
- Noise wave generation (LFSR noise mode and Triangle noise mode).
- Two DAC channels in concurrent mode.
- Generating comparator reference input voltage.
- Output can connect to analog output pin.
- DAC conversion can be enabled by EVIC signals.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be configured to left-aligned or right-aligned mode. The voltage can be used for comparator reference input voltage and analog output voltage.

The DAC channels can work independently or concurrently.

3.17. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Configurable analog input source.
- Outputs to I/O.
- Outputs to timers for triggering.
- Outputs to EXTI.
- Outputs to NVIC.
- Outputs to POC.
- Outputs to GTOC.
- Outputs to EVIC.

- Digital noise filter.

The general purpose comparators can work either standalone (all terminal are available on I/Os) or together with the timers.

It can be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieve some current control by working together with a PWM output of a timer and the DAC.

3.18. Event interconnection unit (EVIC)

- Supports different optional event source;
- Peripheral has its own register to select event source;
- Event signal can be generated by external pin input detection or output of other peripherals;
- Event trigger operation for I/O pins status.

The event interconnection unit (EVIC) allows software to select event signals generated by various peripheral modules for a variety of applications. EVIC provides a flexible mechanism for a peripheral to select different event source. Therefore, the different modules are interconnected to each other through EVIC.

3.19. Space Vector Pulse Width Modulation (SVPWM)

The SVPWM main features are as follows:
The algorithm includes seven-stage PWM and five-stage PWM.
The three phase PWM wave is generated directly with the voltage space vector.
Float point operation.
Support synthetic voltage vector overmodulation processing.

The SVPWM（Space Vector Pulse Width Modulation）calculation unit is used to control the AC induction motor or permanent magnet synchronous motor in the three-phase voltage source inverter power device of special Switch trigger sequence and the combination of pulse width.This Switch trigger sequence and combination will produce three sinusoidal currents in the stator coil with an electrical angle difference of 120°.

3.20. TIMER

Advanced timer (TIMERx, x=0, 7)

- Total channel num: 8.
- Counter width: 16 bits.
- Selectable clock source: internal clock, internal trigger, external input, external trigger.
- Multiple counter modes: up counting, down counting and center-aligned counting.
- Quadrature decoder: used for motion tracking and determination of both rotation direction

and position.

- Hall sensor function: used for 3-phase motor control.
- Programmable prescaler: 16 bits. The factor can be changed ongoing.
- Each channel is independent and user-configurable: input capture mode, output compare mode, programmable PWM mode, single pulse mode and trigger out.
- Programmable dead time insertion.
- Auto reload function.
- Programmable counter repetition function.
- Break input function.
- Interrupt output or DMA request: update event, trigger event, compare/capture event and break input.
- Daisy chaining of timer module allows a single timer to start multiple timers.
- Timer synchronization allows the selected timers to start counting on the same clock cycle.
- Timer master-slave management.

The advanced timer module (TIMER0/7) is an eight-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The advanced timer has a 16-bit counter that can be used as an unsigned counter.

In addition, the advanced timers can be programmed and be used for counting, their external events can be used to drive other timers.

Timer also includes a dead-time insertion module which is suitable for motor control applications.

Timers are completely independent with each other, but they may be synchronized to provide a larger timer with their counter value increasing in unison.

General level0 timer (TIMERx, x=1,2)

- Total channel num: 4.
- Counter width: 16 bits.
- Selectable clock source: internal clock, internal trigger, external input, external trigger.
- Multiple counter modes: up counting, down counting and center-aligned counting.
- Quadrature decoder: used for motion tracking and determination of both rotation direction and position.
- Hall sensor function: used for 3-phase motor control.
- Programmable prescaler: 16 bits. The factor can be changed ongoing.
- Each channel is user-configurable: input capture mode, output compare mode, programmable PWM mode and single pulse mode.
- Auto reload function.
- Interrupt output or DMA request: update event, trigger event and compare/capture event.
- Daisy chaining of timer module allows a single timer to start multiple timers.
- Timer synchronization allows the selected timers to start counting on the same clock cycle.

- Timer master-slave management.

The general level0 timer module (TIMER1/2) is a four-channel timer that supports input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level0 timer has a 16-bit counter that can be used as an unsigned counter.

In addition, the general level0 timers can be programmed and be used for counting, their external events can be used to drive other timers.

Timers are completely independent with each other, but they may be synchronized to provide a larger timer with their counter value increasing in unison.

3.21. General purpose timer (GPTIMER)

- Total channel num: 2.
- Counter width: 16 bits.
- Selectable clock source: internal clock, external trigger.
- Multiple counter modes: up counting, down counting and center-aligned counting.
- Programmable prescaler: 16 bits. The factor can be changed ongoing.
- Each channel is independent and user-configurable: input capture mode, output compare mode, programmable PWM mode, single pulse mode.
- Auto reload function.
- Programmable counter repetition function.
- Interrupt output or DMA request: counter reset event, trigger event, compare/capture event.
- Synchronous start/stop/reset of multiple timers can be triggered by EVIC, channel input and ETI input
- Timer synchronization allows selected timers to start counting at the same tick period.
- The ADC triggers the request output and the pin monitoring, and has the repeat skip function.
- Global updates.
- Complementary output and dead-time insertion (asymmetric).
- Work with GTOC to achieve stop output function.
- External pulse width measurement

The general purpose timer module (GPTIMER0/1) is two-channel timer that supports both input capture and output compare. They can generate PWM signals to be used for power factor correction (PFC). The general purpose timer has a 16-bit counter that can be used as an unsigned counter.

In addition, the general purpose timers can be programmed and be used for counting, their external events can be used to drive other timers.

Timers are completely independent with each other, but they may be synchronized to provide a larger timer with their counter value increasing in unison (Through the EVIC function).

3.22. Compare timer W(CPTIMERW)

- Counter width: 32-bit or 16-bit configurable.
- Clock source: internal clock only.
- Counter mode: count up only.
- Auto reload function.
- Programmable prescaler: 16-bits. Factor can be changed on the go.
- Counter clear function: counter clear at input capture.
- Input capture: 2x input channels with edge programmable
- Compare match: 4x compare channels with 2 channels pulse output supported.
- EVIC interconnect input: counter enable, counter restart and event count.
- EVIC interconnect output: compare match event regarless of interrupt enable bit.
- Interrupt generated at input capture, compare match and update event.

The compare timer W module contains a 32-bit unsigned counter which can be configured to 16-bit. The compare timer W has two input capture channels and four compare match channels with 2 channels pulse output supported. All the channels and counter update event can be configured to generate interrupt or EVIC event at set period.

3.23. Compare timer (CPTIMER)

- Total counters: 2 counters each module.
- Counter width: 16-bit.
- Clock source: internal clock only.
- Counter mode: count up only.
- Programmable prescaler: 16-bits. Factor can be changed on the go.
- Auto reload function.
- Counter oveflow event output to EVIC for trigger.
- Interrupt generate at update event.

The compare timer module (CPTIMER0/1) has two independent 16-bit unsigned counters, two modules total 4 counters. The compare timer can be configured to generate interrupt or EVIC request at set period.

3.24. Universal asynchronous receiver / transmitter (UART)

- NRZ standard format
- Full duplex communication
- Half duplex single wire communications
- Programmable baud-rate generator
  - Divided from the peripheral clocks, PCLK1 for UART0/1/2/3.
  - Oversampling by 8 or 16

  - Maximum speed up to 12 MBits/s (PCLK1 96M and oversampling by 8)
- Fully programmable serial interface characteristics:
  - Even, odd or no-parity bit generation/detection
  - A data word length can be 7, 8, 9 or 10 bits
  - 1 or 2 stop bit generation
- Transmitter and receiver can be enabled separately
- DMA request for data buffer access
- LIN break generation and detection
- IrDA support
- Multiprocessor communication
  - Enter into mute mode if address match does not occur
  - Wake up from mute mode by idle frame or address match detection
- Various status flags:
  - Flags for transfer detection: receive buffer not empty (RBNE), transmit buffer empty (TBE), transfer complete (TC), and busy (BSY).
  - Flags for error detection: overrun error (ORERR), noise error (NERR), frame error (FERR) and parity error (PERR)
  - Flag for LIN mode: LIN break detected (LBDF)
  - Flag for multiprocessor communication: IDLE frame detected (IDLEF)
  - Interrupt occurs at these events when the corresponding interrupt enable bits are set

The Universal Asynchronous Receiver / Transmitter (UART) provides a flexible serial data exchange interface. Data frames can be transferred in full duplex or half duplex mode, asynchronously through this interface. A programmable baud rate generator divides the PCLK1 to produce a dedicated baud rate lock for the UART transmitter and receiver.

Besides the standard asynchronous receiver and transmitter mode, the UART implements several other types of serial data exchange modes, such as IrDA (infrared data association) SIR mode, LIN (local interconnection network) mode. It also supports multiprocessor communication mode. The data frame can be transferred from LSB or MSB bit. The polarity of the data bits and the TX / RX pins can be configured independently and flexibly.

ALL UARTs support DMA function for high-speed data communication.

3.25. Inter-integrated circuit (I2C)

- Parallel-bus to I2C-bus protocol converter and interface.
- Both master and slave functions with the same interface.
- Bi-directional data transfer between master and slave.
- Supports 7-bit and 10-bit addressing and general call addressing.
- Multiple 7-bit slave addresses (2 address, configurable mask).
- Programmable setup time and hold time.
- Multi-master capability.

- Supports standard mode (up to 100 KHz) and fast mode (up to 400 KHz) and fast mode plus (up to 1MHz, I2CFMPEN (fast mode plus) must be enabled in SYSCFG_CFG1 of SYSCFG module).
- Configurable SCL stretching in slave mode.
- Supports DMA mode.
- SMBus 3.0 and PMBus 1.3 compatible.
- Configure the SMBEN bit in I2C_CTL0 to control whether I2C works in SMBus mode.
- Optional PEC (packet error checking) generation and check.
- Programmable digital noise filters.
- Wakeup from Sleep mode and Deep-sleep mode on I2C address match.
- Independent clock from PCLK.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL.

The I2C interface implements standard I2C protocol with standard mode, fast mode and fast mode plus as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus). It also supports multi-master I2C bus. The I2C interface provides DMA mode for users to reduce CPU overload.

3.26. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex or half-duplex or simplex mode.
- Separate transmit and receive buffer, 16 bits wide.
- Data frame size can be 8 or 16 bits.
- Bit order can be LSB or MSB.
- Software and hardware NSS management.
- Hardware CRC calculation, transmission and checking.
- Transmission and reception using DMA.
- SPI TI mode supported.
- SPI NSS pulse mode supported.
- Quad-SPI configuration available in master mode.

The SPI module can communicate with external devices using the SPI protocol.

The serial peripheral interface (SPI) provides a SPI protocol of data transmission and reception function in master or slave mode. Both full-duplex and simplex communication modes are supported, with hardware CRC calculation and checking. Quad-SPI master mode is supported.

3.27. Controller area network (CAN)

- Supports CAN protocols version 2.0A, B.

- Baud rates up to 1 Mbit/s.
- Supports the time-triggered communication.
- Interrupt enable and clear.

Transmission

- Supports 3 transmit mailboxes.
- Supports priority of transmission message.
- Supports time stamp at SOF transmission.

Reception

- Supports 2 Rx FIFOs and each has 3 messages depth.
- 28 scalable/configurable identifier filter banks.
- FIFO lock.

Time-triggered communication

- Disable retransmission automatically in time-triggered communication mode.
- 16-bit free timer.
- Time stamp on SOF reception.
- Time stamp sent in last two data bytes.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer.

As CAN network interface, basic extended CAN supports the CAN protocols version 2.0A and B. The CAN interface automatically handles the transmission and the reception of CAN frames. The CAN provides 28 scalable/configurable identifier filter banks in GD32M531xx. The filters are used for selecting the input message as software requirement and otherwise discarding the message. Three transmit mailboxes are provided to the software for transfer messages. The transmission scheduler decides which mailbox will be transmitted firstly. Three complete messages can be stored in every FIFO. The FIFOs are managed completely by hardware. Two receiving FIFOs are used by hardware to store the incoming messages. In addition, the CAN controller provides all hardware functions, which supports the time-triggered communication option, in safety-critical applications.

3.28. Package and operation temperature

- LQFP48(GD32M531CxTx), LQFP64 (GD32M531RxTx)
- Operation temperature range: -40°C to +105°C (industrial level)

4. Electrical characteristics

4.1. Parameter introduction

- Parameter conditions: Unless otherwise specified, all values given for V_{DD} = V_{DDA}/V_{REFP} = 5.0V, T_A = 25°C, and all voltages are referenced to Vss.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from design or simulation and/or process characteristics.
- Value guaranteed by sample, not 100% tested in production indicates that the value is derived from testing parameters with a small sample size.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from comprehensive evaluation after random test, and the sample size for random test comes from a batch of samples (the sample size of which is specified in JESD47K).
- If the value is not specially indicated, it means the value guaranteed by 100% tested in production.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
USB	Universal Serial Bus
SPI	Serial Peripheral Interface
TMU	Trigonometric Math Unit
SVPWM	Space Vector Pulse Width Modulation
I2C	Inter-integrated circuit interface
POC	Port Output Controller
GTOC	GPTIMER Output Controller

4.2. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly beyond the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)

Symbol	Description	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS}-0.3	V_{SS}+5.9	V
V_{DDA}/V_{REFP}	External analog supply voltage(3)	V_{SSA}/V_{REFN}-0.3	V_{SSA}/V_{REFN}+5.9	V
V_{IN}	Input voltage on PF8,PF9,PF10	V_{SS}-0.3	V_{SS}+5.9	V
	PD2,PD4,PD5,PC0~PC12	V_{SS}-0.3	V_{DDA2}/V_{REFP2} +0.3	
	Other than above	V_{SS}-0.3	V_{DD}+0.3	
$\lvert\Delta V_{DD}\rvert$	Variations between different power supply pins of V_{DD} power domain	—	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	20	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	110	
I_{DD}	Maximum current into each VDD pin	—	100	
I_{SS}	Maximum current into each VSS pin	—	100	
I_{INJ}	Injected current on each GPIO pin	—	-5/+0	
$\sum \lvert I_{INJ}\rvert$(4)	Total injected current on all GPIO pins	—	25	
T_{STG}	Storage temperature range	-55	125	°C
T_J	Maximum junction temperature	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

(4) When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ}|$ is the absolute sum of the negative injected currents (instantaneous values).

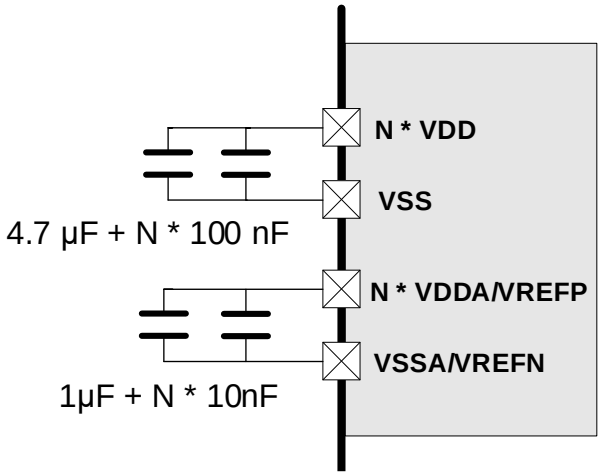
4.3. Operating conditions characteristics

Table 4-3. General operating conditions(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.7	5.0	5.5	V
V_{DDA}/V_{REFP}	Analog supply voltage	Same as V_{DD}	2.7	5.0	5.5	V
V_{CORE}	Core logic supply voltage powered by internal voltage regulator	—	—	1.25	—	V
f_{HCLK}	AHB clock frequency	—	—	—	180	MHz
f_{APB1}	APB1 clock frequency	—	—	—	90	
f_{APB2}	APB2 clock frequency	—	—	—	180	
P_D	Power dissipation at T_A = 105°C of LQFP64	—	—	—	386	mW
	Power dissipation at T_A = 105°C of LQFP48	—	—	—	311	mW
T_A	Operating temperature range	—	-40	—	105	°C
T_J	Junction temperature range	—	-40	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-1. Recommended power supply decoupling capacitors(1)



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

4.4. Power supply requirement characteristics

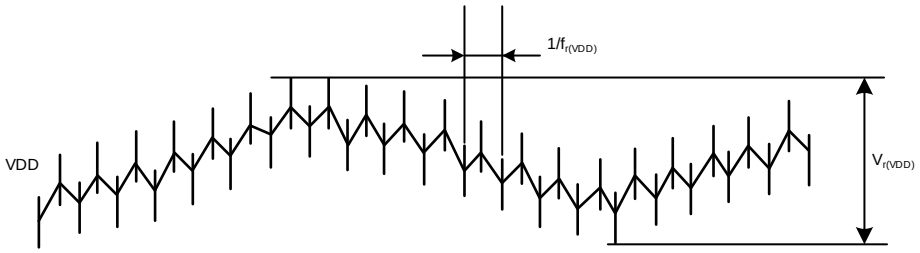
Table 4-4. Power supply requirement characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	At normal startup	0	∞	μs/V
	V_{DD} fall time rate	—	50	∞	
$t_{VDDA/VREFP}$	V_{DDA}/V_{REFP} rise time rate	At normal startup	0	∞	
	V_{DDA}/V_{REFP} fall time rate	—	50	∞	
$f_{R(VDD)}$	Allowable ripple frequency	$V_{R(VDD)} \leq 0.2\ V_{DD}$	—	10	kHz
		$V_{R(VDD)} \leq 0.08\ V_{DD}$	—	1	MHz
		$V_{R(VDD)} \leq 0.06\ V_{DD}$	—	10	
ΔV_{DD}(2)	Allowable voltage change rising and falling gradient	When V_{DD} change exceeds V_{DD} ± 10%	1	—	ms/V

(1) Value guaranteed by design, not 100% tested in production.

(2) The ripple voltage must meet the allowable ripple frequency $f_{R(VDD)}$ within the range between the V_{DD} upper limit (5.5V) and lower limit (2.7V). When the V_{DD} change exceeds V_{DD} ± 10%, the allowable voltage change rising and falling gradient dt/dV_{DD} must be met.

Figure 4-2. Rise and fall gradient and ripple frequency characteristics



4.5. Start-up timings of Operating conditions

Table 4-5. Start-up timings of Operating conditions (1)(2)(3)(4)

Symbol	Description	Conditions	Typ	Unit
t_{ST}	Start-up time	Clock source from IRC32M	15.36	ms

(1) Value guaranteed by sample, not 100% tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.

(3) PLL is off.

(4) Excluding the time to initialize SRAM during startup.

4.6. Wake-up times from power saving modes

Table 4-6. Wake-up time from power saving modes(1)(2)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{Sleep}	Wakeup from Sleep mode	—	—	0.75		μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode	—	—	35.07	—	μs
$t_{Standby}$	Wakeup from Standby mode	—	—	0.43	—	ms

(1) Value guaranteed by sample, not 100% tested in production.

(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: V_{DD} = V_{DDA} = 5.0 V, IRC32M = System clock = 32 MHz.

4.7. Power consumption

The power consumption is measured as described in ***Figure 4-3. Power consumption measurement diagram***. The current consumption values are derived from the tests powered by V_{DD} = V_{DDA}, while the current is I_{SUM}. Unless otherwise stated, V_{DD} = V_{DDA} =5.0 V is applied to supply pins in typical current consumption columns, and V_{DD} = V_{DDA} = 5.5V is applied in maximum current consumption columns.

The MCU is configured under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- Configure the WSCNT bits in the FMC_WS register correctly depend on the AHB clock frequency (refer to the table “The relation between WSCNT and AHB clock frequency” available in the GD32M531_User_Manual).

Figure 4-3. Power consumption measurement diagram

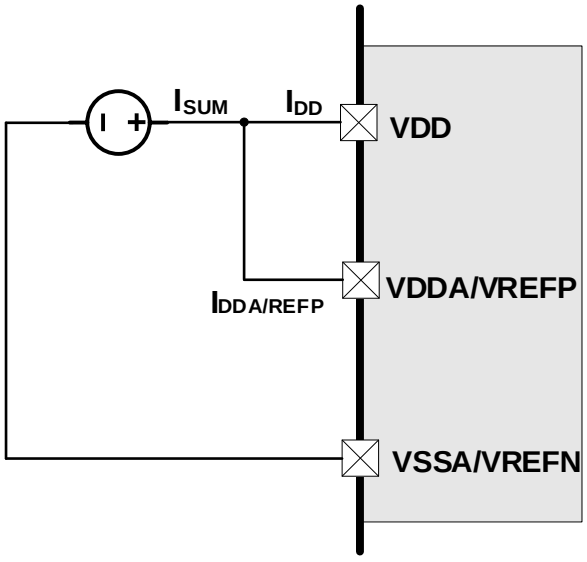


Table 4-7. Power consumption in Run mode(1)(2)(3)

Symbol	Description	Conditions			Typ					Max(4)			Unit
		Execute from	General	f_{HCLK1}	-40°C	25°C	55°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Run mode)	EFLASH	HXTAL = 8 MHz, PLL on, System clock = f_{HCLK1}	180 MHz	33.363	34.217	35.578	38.892	43.118	TBD	TBD	TBD	mA
				168 MHz	31.180	31.993	33.324	36.546	40.682	TBD	TBD	TBD	
				120 MHz	22.419	23.139	24.353	27.298	31.229	TBD	TBD	TBD	
				72 MHz	13.758	14.384	15.489	18.221	21.890	TBD	TBD	TBD	
				32 MHz	6.422	6.986	7.996	10.581	14.075	TBD	TBD	TBD	
				8 MHz	2.009	2.527	3.495	6.018	9.495	TBD	TBD	TBD	
			IRC32M = 32 MHz, PLL on, System clock = f_{HCLK1}	180 MHz	32.614	33.512	35.156	37.969	42.149	TBD	TBD	TBD	
				168 MHz	30.491	31.349	32.986	35.733	39.796	TBD	TBD	TBD	
				120 MHz	22.014	22.787	24.315	26.876	30.708	TBD	TBD	TBD	
				72 MHz	13.579	14.260	15.695	18.257	21.746	TBD	TBD	TBD	
				32 MHz	6.532	7.144	8.513	10.927	14.289	TBD	TBD	TBD	
		SRAM	HXTAL = 8 MHz, PLL on, System clock = f_{HCLK1}	180 MHz	23.693	24.561	25.827	28.859	32.820	TBD	TBD	TBD	
				168 MHz	22.142	22.988	24.243	27.204	31.083	TBD	TBD	TBD	
				120 MHz	15.955	16.696	17.872	20.664	24.360	TBD	TBD	TBD	
				72 MHz	9.878	10.521	11.618	14.271	17.829	TBD	TBD	TBD	
				32 MHz	4.705	5.267	6.305	8.854	12.310	TBD	TBD	TBD	
				8 MHz	1.589	2.105	3.101	5.602	9.021	TBD	TBD	TBD	
			IRC32M = 32 MHz, PLL on, System clock = f_{HCLK1}	180 MHz	24.066	24.974	26.587	29.387	33.181	TBD	TBD	TBD	
				168 MHz	22.515	23.391	24.985	27.727	31.463	TBD	TBD	TBD	
				120 MHz	16.320	17.091	18.611	21.196	24.774	TBD	TBD	TBD	
				72 MHz	10.163	10.833	12.280	14.743	18.185	TBD	TBD	TBD	
				32 MHz	5.019	5.609	6.992	9.392	12.921	TBD	TBD	TBD	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) All peripherals are disabled except when explicitly mentioned.

(4) V_{DD} = V_{DDA} = 5.5 V for values in Max columns.

Table 4-8. Power consumption in Run mode with different codes(1)(2)(3)

Symbol	Description	Conditions			Typ	Unit	Typ	Unit
		General	Execute from	Code				
I_{SUM}	Sum of supply current from VDD and VDDA	IRC32M = 32 MHz, PLL on, System clock = 180 MHz, f_{HCLK1} = 180 MHz, All peripherals disabled	EFLASH	Coremark	44.5	mA	247.22	µA /MHz
				Dhrystone	42.6		236.67	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) The pre-fetch buffer, I-cache and D-cache are enabled when fetching from EFLASH.

Table 4-9. Power consumption in Sleep mode(1)(2)

Symbol	Description	Conditions		Typ					Max(3)			Unit
		General	f_{HCLK1}	-40°C	25°C	55°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Sleep mode)	HXTAL = 8 MHz, PLL on, System clock = f_{HCLK1}	180 MHz	7.87	8.54	9.91	12.62	16.63	TBD	TBD	TBD	mA
			168 MHz	7.38	8.03	9.40	12.12	16.13	TBD	TBD	TBD	
			120 MHz	5.40	6.02	7.37	10.06	14.02	TBD	TBD	TBD	
			72 MHz	3.91	4.51	5.84	8.50	12.43	TBD	TBD	TBD	
			32 MHz	2.05	2.62	3.92	6.54	10.44	TBD	TBD	TBD	
			8 MHz	0.91	1.50	2.78	5.37	9.25	TBD	TBD	TBD	
		RC32M = 32 MHz, PLL on, System clock = f_{HCLK1}	180 MHz	8.21	8.90	10.28	12.96	17.02	TBD	TBD	TBD	
			168 MHz	7.71	8.40	9.79	12.46	16.73	TBD	TBD	TBD	
			120 MHz	5.75	6.39	7.76	10.39	14.43	TBD	TBD	TBD	
			72 MHz	3.82	4.44	5.78	8.37	12.37	TBD	TBD	TBD	

Symbol	Description	Conditions		Typ					Max(3)			Unit
		General	f_{HCLK1}	-40°C	25°C	55°C	85°C	105°C	25°C	85°C	105°C	
			32 MHz	2.21	2.79	4.13	6.70	10.66	TBD	TBD	TBD	
			8 MHz	1.47	2.06	3.37	5.93	9.86	TBD	TBD	TBD	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) V_{DD} = V_{DDA} = 5.5 V for values in Max columns.

Table 4-10. Power consumption in Deep-sleep mode(1)(2)

Symbol	Description	Conditions		Typ					Max(3)			Unit
		General	V_{DD}	-40°C	25°C	55°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Deep-sleep mode)	LDO output voltage is 0.9V, IRC32K off	2.7V	0.171	0.373	0.919	2.095	3.820	TBD	TBD	TBD	mA
			3.3V	0.174	0.376	0.923	2.105	3.830	TBD	TBD	TBD	
			5.0V	0.185	0.387	0.939	2.130	3.915	TBD	TBD	TBD	
			5.5V	0.196	0.396	0.950	2.175	3.995	TBD	TBD	TBD	
		LDO output voltage is 1.0V, IRC32K off	2.7V	0.178	0.444	1.129	2.560	4.645	TBD	TBD	TBD	mA
			3.3V	0.180	0.447	1.135	2.575	4.680	TBD	TBD	TBD	
			5.0V	0.191	0.459	1.155	2.615	4.790	TBD	TBD	TBD	
			5.5V	0.199	0.469	1.169	2.650	4.875	TBD	TBD	TBD	
		LDO output voltage is 1.1V, IRC32K off	2.7V	0.188	0.539	1.395	3.150	5.660	TBD	TBD	TBD	mA
			3.3V	0.191	0.542	1.399	3.160	5.685	TBD	TBD	TBD	
			5.0V	0.202	0.554	1.420	3.210	5.815	TBD	TBD	TBD	
			5.5V	0.211	0.563	1.437	3.265	5.920	TBD	TBD	TBD	
		LDO output voltage is 1.2V, IRC32K off	2.7V	0.202	0.658	1.737	3.905	6.940	TBD	TBD	TBD	mA
			3.3V	0.205	0.663	1.745	3.925	6.995	TBD	TBD	TBD	
			5.0V	0.216	0.677	1.771	3.995	7.150	TBD	TBD	TBD	
			5.5V	0.224	0.687	1.789	4.050	7.225	TBD	TBD	TBD	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) V_{DD} = V_{DDA} = 5.5 V for values in Max columns.

Table 4-11. Power consumption in Standby mode(1)(2)

Symbol	Description	Conditions		Typ					Max(3)			Unit
		General	V_{DD}	-40°C	25°C	55°C	85°C	105°C	25°C	85°C	105°C	
I_{SUM}	Sum of supply current from VDD and VDDA (Standby mode)	IRC32K on, FWDGT on	2.7V	1.96	2.29	3.82	8.62	18.08	TBD	TBD	TBD	µA
			3.3V	2.20	2.62	4.19	9.47	19.65	TBD	TBD	TBD	
			5.0V	2.97	3.80	6.09	13.15	26.60	TBD	TBD	TBD	
			5.5V	3.27	4.35	7.02	15.09	30.00	TBD	TBD	TBD	
		IRC32K off, FWDGT off	2.7V	1.45	1.77	3.23	8.00	17.35	TBD	TBD	TBD	
			3.3V	1.65	2.00	3.66	8.72	18.82	TBD	TBD	TBD	
			5.0V	2.18	2.78	5.06	12.03	25.22	TBD	TBD	TBD	
			5.5V	2.36	3.34	6.05	14.01	28.81	TBD	TBD	TBD	

(1) Value guaranteed by sample, not 100% tested in production.

(2) During power consumption test, GPIO needs to be configure as Analog Input mode.

(3) V_{DD} = V_{DDA} = 5.5 V for values in Max columns.

The current consumption of the on-chip peripherals is given in the following table. To avoid adding the CPU dynamic power consumption to the peripheral power consumption, the MCU needs to enter sleep mode to stop the CPU operation during current measurement. The MCU is configured under the following conditions:

• All I/O pins are in analog input mode

• The given value is in the table calculated by measuring the difference of the current consumptions:

-- The target peripheral is clocked on and enters sleep mode

-- All peripherals are clocked off and enter sleep mode

The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

The values in the table are equal to the peripheral current divided by the clock frequency of the corresponding BUS.

Table 4-12. Peripheral current consumption characteristics(1)(2)

Peripherials		Typical consumption	Unit
APB1	DAC0	1.03	μA/MHz
	PMU	10.43	
	CFMU	0.34	
	I2C	5.41	
	UART3	1.89	
	UART2	1.89	
	UART1	1.88	
	UART0	1.86	
	WWDGT	0.32	
	CPTIMERWEN	2.68	
	CPTIMER1EN	1.23	
	CPTIMER0EN	1.34	
APB2	CAN	4.44	
	EVIC	1.54	
	GPTIMER1	6.97	
	GPTIMER0	7.04	
	TIMER2	3.96	
	TIMER1	3.89	
	TIMER7	11.69	
	SPI	0.84	
	TIMER0	11.64	
	ADC2	5.94	
	ADC0	4.69	
	CMP	0.89	

Peripherials		Typical consumption	Unit
	CFGEN	3.69	
AHB	TMU	1.43	
	SVPWM	0.70	
	GTOCE	1.34	
	POC	2.62	
	GPION	0.59	
	GPIOG	0.37	
	GPIOF	0.52	
	GPIOE	0.56	
	GPIOD	0.64	
	GPIOC	0.80	
	GPIOB	0.39	
	GPIOA	0.33	
	CRC	0.46	
	DMAMUX	3.68	
	SRAMSP	1.79	
	DMA1	3.42	
	DMA0	3.54	

(1) Value guaranteed by sample, not 100% tested in production.

(2) System clock = f_{HCLK} = 180 MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}.

4.8. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-13. System level ESD and EFT characteristics***(1). System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-13. System level ESD and EFT characteristics(1) (2)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 5 V, T_A = 25 °C, f_{HCLK} = 180 MHz IEC 61000-4-2	LQFP64	CD 8KV AD 15KV	4A
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 5 V, T_A = 25 °C, f_{HCLK} =180 MHz IEC 61000-4-4	LQFP64	4KV	4A

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the evaluation methods for system-level ESD and system-level EFT test methods and test levels can be referred to in AN127 and AN128.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-14. EMI characteristics***, The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3 standard which specifies the test board and the pin loading.

Table 4-14. EMI characteristics(1) (2)

Symbol	Description	Conditions	Package	Max vs. [f_{HXTAL}/f_{HCLK}] 8/180 MHz			Unit
				0.1-30MHz	30-130MHz	130MHz-1GHz	
S_{EMI}	Peak level	V_{DD} = 5.5 V, T_A = 25 °C, f_{HCLK} = 180 MHz, conforms to SAE J1752-3	LQFP64	9.52	12.98	19.93	dBµV

(1) Value guaranteed by sample, not 100% tested in production.

(2) The explanation of the chip-level EMI test methods can be referred to in AN125.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Latch-up (LU, according to JESD78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-14. Component level ESD characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	JS-001	LQFP64	4000	V	3A
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	JS-002	LQFP64	1000	V	C3
LU	I-test	T_A = 125 °C; JESD78	LQFP64	200	mA	Class II Level A
	V_{supply} over voltage			8.25	V	

(1) Value guaranteed by sample, not 100% tested in production.

4.9. Power supply supervisor characteristics

Table 4-15. Power supply supervisor characteristics(1)

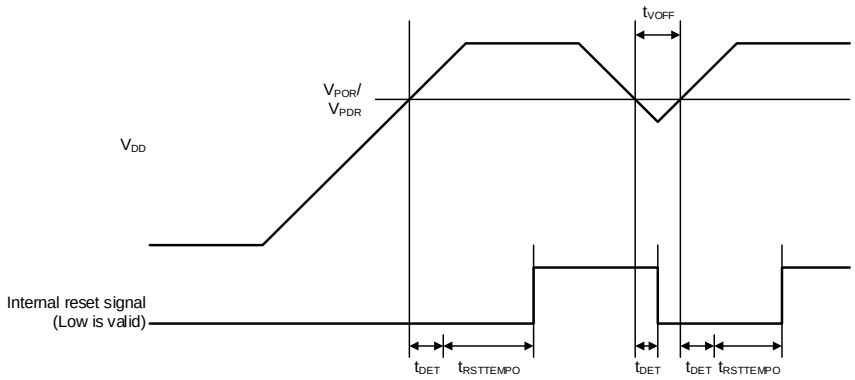
Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LVD0}	Low voltage	VDSEL<1:0> = 10(rising edge)	—	2.90	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
	Detector level selection	VDSEL<1:0> = 10(falling edge)	—	2.82	—	
		VDSEL<1:0> = 11(rising edge)	—	4.31	—	
		VDSEL<1:0> = 11(falling edge)	—	4.23	—	
V_{LVD1}		LVD1T<3:0> = 0100(rising edge)	—	4.62	—	
		LVD1T<3:0> = 0100(falling edge)	—	4.54	—	
		LVD1T<3:0> = 0101(rising edge)	—	4.55	—	
		LVD1T<3:0> = 0101(falling edge)	—	4.47	—	
		LVD1T<3:0> = 0110(rising edge)	—	4.40	—	
		LVD1T<3:0> = 0110(falling edge)	—	4.32	—	
		LVD1T<3:0> = 1010(rising edge)	—	3.03	—	
		LVD1T<3:0> = 1010(falling edge)	—	2.95	—	
		LVD1T<3:0> = 1011(rising edge)	—	2.96	—	
		LVD1T<3:0> = 1011(falling edge)	—	2.88	—	
V_{LVD2}		LVD2T<3:0> = 0100(rising edge)	—	4.62	—	
		LVD2T<3:0> = 0100(falling edge)	—	4.54	—	
		LVD2T<3:0> = 0101(rising edge)	—	4.55	—	
		LVD2T<3:0> = 0101(falling edge)	—	4.47	—	
		LVD2T<3:0> = 0110(rising edge)	—	4.40	—	
		LVD2T<3:0> = 0110(falling edge)	—	4.32	—	
		LVD2T<3:0> = 1010(rising edge)	—	3.03	—	
		LVD2T<3:0> = 1010(falling edge)	—	2.95	—	
		LVD2T<3:0> = 1011(rising edge)	—	2.96	—	
		LVD2T<3:0> = 1011(falling edge)	—	2.88	—	
$V_{HYST(LVD)}$	LVD hysteresis	—	—	80	—	mV
V_{POR}	Power on reset threshold	—	—	2.58	—	V
V_{PDR}	Power down reset threshold	—	—	2.53	—	V
$V_{HYST(POR\_PDR)}$	POR_PDR hysteresis	—	—	50	—	mV

Symbol	Description	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$	Power on reset temporization	—	—	15.5	—	ms
t_{LVD0}	LVD0 reset temporization	—	—	2	—	µs
t_{LVD1}	LVD1 reset temporization	—	—	2.016	—	
t_{LVD2}	LVD2 reset temporization	—	—	2.016	—	
t_{VOFF}	VDD down time	—	200	—	—	µs
t_{DET}	Response delay time	—	—	—	5	µs
$t_{D(E-A)}$	LVD operation stabilization time (after LVD is enabled)	—	—	—	20	µs

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-4. POR / PDR waveform(1)(2)



(1) The state of the internal reset signal can be approximated by monitoring the GPIO flag value. By measuring the time difference between the V_{POR} and the low-to-high transition of the GPIO flag, the sum of t_{DET} and $t_{RSTTEMPO}$ can be roughly validated.

(2) The voltage on the NRST pin does not strictly equate to the internal reset signal state.

Figure 4-5. Voltage Detection Circuit Timing (V_{LVD0})

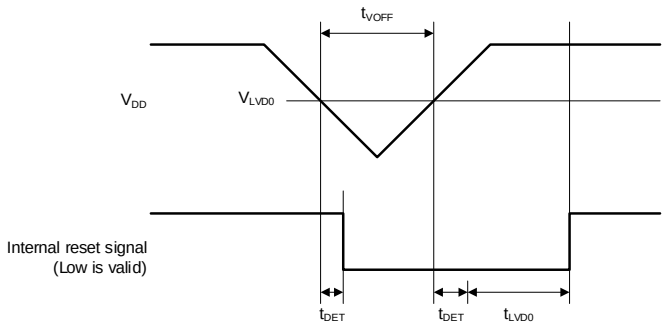


Figure 4-6. Voltage Detection Circuit Timing (V_{LVD1})

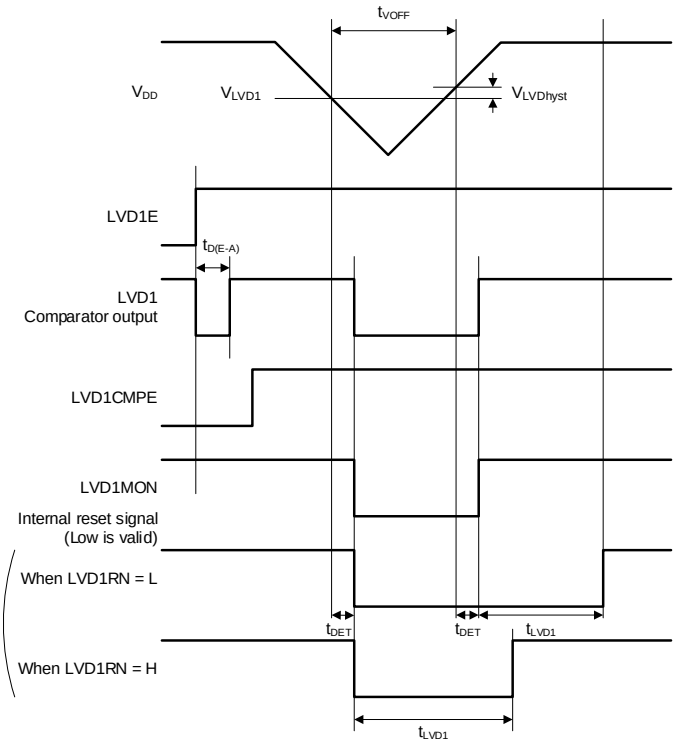
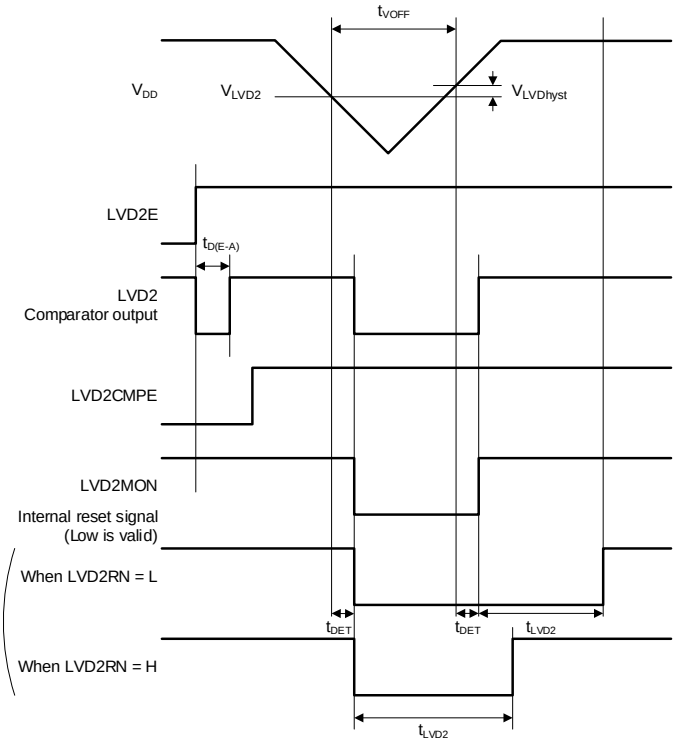
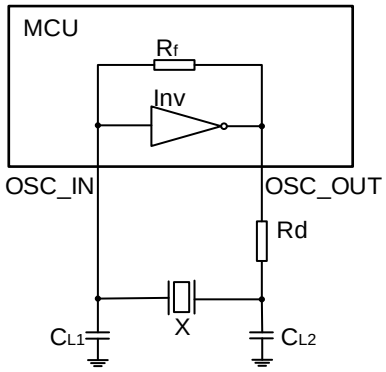


Figure 4-7. Voltage Detection Circuit Timing (V_{LVD2})



4.10. External clock characteristics

Figure 4-8. Internal structure diagram of OSCIN and OSCOUT pin



It is strongly recommended to meature the oscillation allowance (negative resistance) in the final target system (layout) to determine which load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

Table 4-16. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	Crystal or ceramic frequency	2.7 V ≤ V_{DD} ≤ 5.5 V	1	—	24	MHz
R_F	Feedback resistor	V_{DD} = 5.0 V	—	800	—	kΩ
C_{HXTAL}(2)	Recommended load capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Ducy_{(HXTAL)}$	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(3)	Oscillator transconductance	Startup	—	16	—	mA/V
$I_{DD(HXTAL)}$	Crystal or ceramic operating current	V_{DD} = 5.0 V, f_{HCLK} = f_{IRC8M} = 8 MHz	—	0.4	—	mA
$t_{ST(HXTAL)}$ (4)	Crystal or ceramic startup time	V_{DD} = 5.0 V, f_{HCLK} = f_{IRC8M} = 8 MHz	—	1	—	ms

(1) Value guaranteed by design, not 100% tested in production.

(2) C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

(3) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

(4) $t_{ST(HXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 8 MHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-17. High speed external clock characteristics (HXTAL in bypass mode) (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
t_{HXTAL_cyc}	External clock source or oscillator input cycle time	2.7 V ≤ V_{DD} ≤ 5.5 V	20	—	—	ns
f_{HXTAL_ext}	External clock source or oscillator frequency	2.7 V ≤ V_{DD} ≤ 5.5 V	—	—	50	MHz

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{HXTALH}	OSCIN input pin high level voltage	V_{DD} = 5.0 V	0.7V_{DD}	—	V_{DD}	V
V_{HXTALL}	OSCIN input pin low level voltage		V_{SS}	—	0.3V_{DD}	V
$t_{H/L(HXTAL)}$	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$	OSCIN rise or fall time	—	—	—	5	ns
C_{IN}	OSCIN input capacitance	—	—	5	—	pF
$Ducy_{(HXTAL)}$	Duty cycle	—	40	—	60	%

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-9. High-speed external clock source AC timing diagram

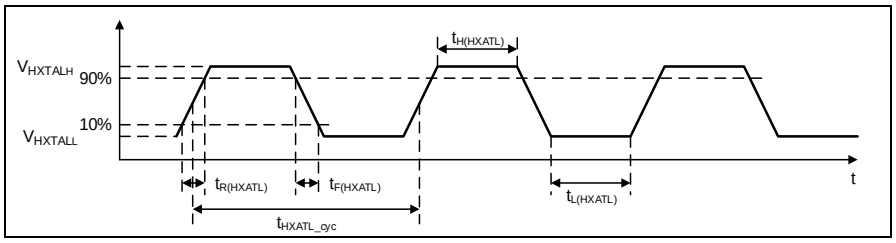
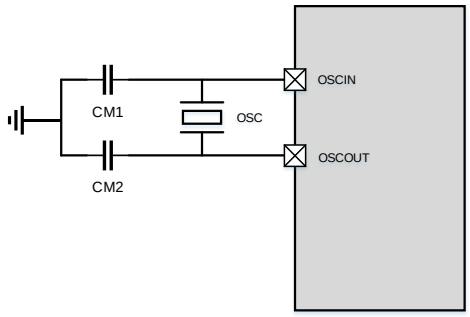


Figure 4-10. Recommended external OSCIN and OSCOUT pins circuit for crystal



4.11. Internal clock characteristics

Table 4-18. High speed internal clock (IRC32M) characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32M}(1)	High Speed Internal Oscillator (IRC32M) frequency	V_{DD} = 5.0 V	—	32	—	MHz
$Drift_{IRC32M}$	IRC32M oscillator Frequency drift, Factory-trimmed(2)	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, T_A = -40 °C ~ +105 °C	-1.5	—	+1.5	%
		V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, T_A = 25 °C	-1	—	+1	
$Trim_{IRC32M}$(1)	IRC32M oscillator User trimming step	—	—	0.3	—	
$Ducy_{IRC32M}$(1)	IRC32M oscillator duty	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V	45	50	55	%

Symbol	Description	Conditions	Min	Typ	Max	Unit
	cycle					
$I_{DDA(IRC32M)}$(1)	IRC32M oscillator operating current	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	400	500	μA
$t_{ST(IRC32M)}$(1)	IRC32M oscillator startup time	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	7.8	10	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by sample, not 100% tested in production.

Table 4-19. Low speed internal clock (IRC32K) characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, T_A = 25 °C	31.2	32	32.8	kHz
		T_A = -40 to 105°C	30.4	—	33.6	
$I_{DDA(IRC32K)}$	IRC32K oscillator operating current	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	0.7	—	μA
$t_{ST(IRC32K)}$	IRC32K oscillator startup time	V_{DD} = V_{DDA}/V_{REFP} = 5.0 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz	—	34	—	μs

(1) Value guaranteed by design, not 100% tested in production.

4.12. PLL characteristics

Table 4-20. PLL characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	4	—	16	MHz
	PLL input clock duty cycle	—	45	—	55	%
f_{PLLOUT}	PLL output clock frequency	—	40	—	200	MHz
f_{VCO}	PLL VCO output clock frequency	—	80	—	400	
t_{LOCK}	PLL lock time	—	151	—	553	μs
I_{DD}	Current consumption on V_{DD}	f_{VCO} = 400 MHz	—	820	—	μA
		f_{VCO} = 80 MHz	—	228	—	
$Jitter_{PLL}$(2)	Cycle to cycle Jitter (rms)	System clock 180Mhz, Measure clock 22.5MHz	—	16.5	—	ps
	Cycle to cycle Jitter (peak to peak)		—	121	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value given with main PLL running.

4.13. CFMU characteristics

Table 4-21. CFMU characteristics(1)(2)(3)

Symbol	Description		Conditions	Min	Max	Unit
$t_{CFMUREF}$	CFMUREF input pulse width	$t_{PBcyc} \leq t_{CFMU}$	—	4.5 t_{CFMU} + 3 t_{PBcyc}	—	ns
		$t_{PBcyc} > t_{CFMU}$	—	5 t_{CFMU} + 6.5 t_{PBcyc}	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) t_{PBcyc}: PCLKB cycle.
(3) t_{CFMU}: CFMU count clock source cycle.

4.14. Memory characteristics

Table 4-22. Flash memory characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_{DD(FLASH)}$ (2)	Average supply current from V_{DD} during FLASH operation	Erasing	—	0.5	—	mA
		Programming	—	0.7	—	
	Max supply current from V_{DD} during FLASH operation	Erasing	—	3.6	—	
		Programming	—	1	—	
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = -40 °C ~ +105 °C	100	—	—	kcycles
t_{RET}(3)	Data retention time	T_A = 85 °C, after up to 0 kcycles(4)	25	—	—	years
		T_A = 105 °C, after up to 0 kcycles(4)	4	—	—	years
		T_A = 85 °C, after up to 10 kcycles(4)	15	—	—	years
t_{PROG}	Four Word programming time	Main Flash	—	153	—	μs
		Data Flash	—	216	—	
t_{PROG_ROW}	One row (32 double word) programming time	Normal programming	—	1.064	1.256	ms
		Fast programming	—	0.89	1.11	
t_{PROG_PAGE}	One page (2 Kbytes) programming time	Normal programming	—	4	6	
		Fast programming	—	3.5	4.5	
t_{PROG_BANK}	One bank (256 Kbyte) programming time	Normal programming	—	1064	1256	
		Fast programming	—	885	1114	
t_{ERASE}	Page erase time	—	—	5.13	—	
t_{MERASE}	Mass erase time	—	—	35	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by sample, not 100% tested in production.
(3) Value guaranteed by characterization, not 100% tested in production.
(4) Cycling performed over the whole temperature range.

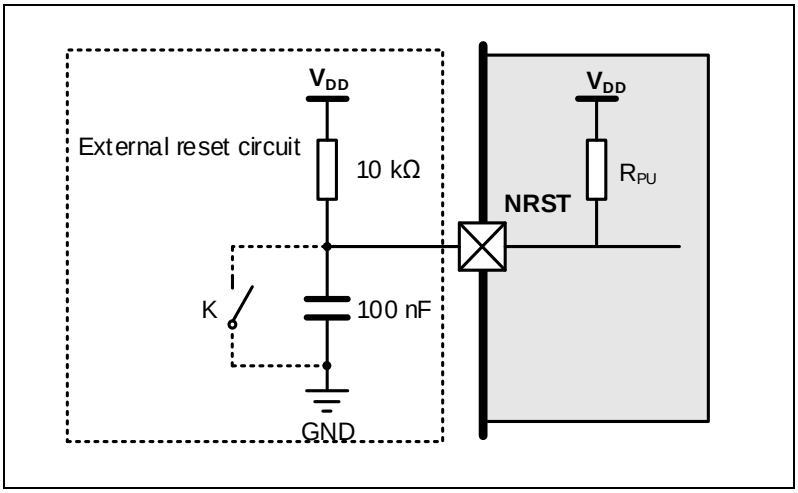
4.15. NRST pin characteristics

Table 4-23. NRST pin characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST Input low level voltage	—	-0.3	—	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST Input high level voltage	—	$0.7V_{DD}$	—	V_{DD}+0.3	
$V_{HYST(NRST)}$	Schmidt trigger Voltage hysteresis	V_{DD} = V_{DDA}/V_{REFP} = 2.7V	—	469	—	mV
		V_{DD} = V_{DDA}/V_{REFP} = 3.3V	—	509	—	
		V_{DD} = V_{DDA}/V_{REFP} = 5.0V		624		
		V_{DD} = V_{DDA}/V_{REFP} = 5.5V	—	654	—	
R_{PU}	Pull-up equivalent resistor	V_{IN} = V_{SS}	—	40	—	kΩ
t_{NRST_F}	Generated filtered reset pulse duration	—	—	—	100	ns
t_{NRST_NF}	Generated not filtered reset pulse duration	—	350	—	—	

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-11. Recommended external NRST pin circuit(1)



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.16. GPIO characteristics

More details about GPIO could be found in ***AN092 GD32 MCU GPIO structure and precautions***.

Table 4-24. I/O static characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{IL(GPIO)}$(1)	All IO Pins Low level input voltage	V_{DD} = 2.7 to 5.5 V, V_{DDA}/V_{REFP} = 3.0 to 5.5 V	—	—	$0.3V_{DD}$	V
$V_{IH(GPIO)}$(1)	All IO Pins High level input voltage	V_{DD} = 2.7 to 5.5 V, V_{DDA}/V_{REFP} = 3.0 to 5.5 V	$0.7V_{DD}$	—	—	V

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{HYS(GPIO)}$(1)	Input hysteresis	V_{DD} = 2.7 to 5.5 V, V_{DDA}/V_{REFP} = 3.0 to 5.5 V	—	585	—	mV
$V_{IL(I2C)}$(1)	I2C pin（SMBus mode）	V_{DD} = 2.7 to 5.5 V	—	—	0.8	V
$V_{IH(I2C)}$(1)	I2C pin（SMBus mode）	V_{DD} = 2.7 to 5.5 V	2.1	—	—	V
I_{LEAK}	Standard IO input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	±2	μA
R_{PU}(1)	Internal pull-up resistor	—	—	40	—	kΩ
R_{PD}(1)	Internal pull-down resistor	—	—	40	—	kΩ
C_{IO}(1)	I/O pin capacitance	I/O pin capacitance	—	3	—	pF

(1) Value guaranteed by design, not 100% tested in production.

Table 4-25. Output voltage characteristics for all I/Os(1)

Symbol	Description	Conditions		Min	Typ	Max	Unit
V_{OL0}(2)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	OSPDx<1:0> = 00 (N5VT_HIA I/O pins，N5VT I/O pins)	V_{DD} = 2.7 V	—	0.32	—	V
			V_{DD} = 5.0 V	—	0.19	—	
			V_{DD} = 5.5 V	—	0.17	—	
V_{OH0}(2)	High level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 2.7 V	—	2.32	—	
			V_{DD} = 5.0 V	—	4.77	—	
			V_{DD} = 5.5 V	—	5.28	—	
V_{OL1}(2)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	OSPDx<1:0> = 01 (N5VT_HIA I/O pins，N5VT I/O pins)	V_{DD} = 2.7 V	—	0.12	—	V
			V_{DD} = 5.0 V	—	0.08	—	
			V_{DD} = 5.5 V	—	0.07	—	
V_{OH1}(2)	High level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 2.7 V	—	2.55	—	
			V_{DD} = 5.0 V	—	4.90	—	
			V_{DD} = 5.5 V	—	5.41	—	
V_{OL2}(2)	Low level output voltage for an IO Pin (I_{IO} = +15 mA)	OSPDx<1:0> = 1x (N5VT_HIA I/O pins)	V_{DD} = 2.7 V	—	0.34	—	V
			V_{DD} = 5.0 V	—	0.21	—	
			V_{DD} = 5.5 V	—	0.20	—	
V_{OH2}(2)	High level output voltage for an IO Pin (I_{IO} = +5 mA)		V_{DD} = 2.7 V	—	2.56	—	
			V_{DD} = 5.0 V	—	4.90	—	
			V_{DD} = 5.5 V	—	5.41	—	
V_{OL5}(3)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	OSPDx<1:0> = 00 (5VT I/O pins)	V_{DD} = 2.7 V	—	0.19	—	V
			V_{DD} = 5.0 V	—	0.12	—	
			V_{DD} = 5.5 V	—	0.11	—	
V_{OH5}(3)	High level output voltage for an IO Pin (I_{IO} = +4 mA)		V_{DD} = 2.7 V	—	2.48	—	
			V_{DD} = 5.0 V	—	4.85	—	
			V_{DD} = 5.5 V	—	5.36	—	
V_{OL6}(3)	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	OSPDx<1:0> = 01 (5VT I/O pins)	V_{DD} = 2.7 V	—	0.10	—	V
			V_{DD} = 5.0 V	—	0.06	—	
			V_{DD} = 5.5 V	—	0.06	—	
V_{OH6}(3)	High level output voltage for an IO Pin		V_{DD} = 2.7 V	—	2.59	—	
			V_{DD} = 5.0 V	—	4.92	—	

Symbol	Description	Conditions		Min	Typ	Max	Unit
	(I_{IO} = +4 mA)		V_{DD} = 5.5 V	—	5.42	—	

(1) Value guaranteed by sample, not 100% tested in production.

(2) The N5VT_HIA I/O pins include PD9–PD14, PE8–PE13, PF13, and PG1. The N5VT I/O pins include other pins except for 5VT I/O pins.

(3) The 5VT I/O pins include PF8-PF10.

Table 4-26. I/O port AC characteristics(1)(2)(3)

IO drive mode	Description	Conditions	Typ	Unit
Normal-drive mode, OSPDx<1:0> = 00	T_{Rise}/T_{Fall}	V_{DD}=2.7V，C_L=30pF	14.63	ns
		V_{DD}=3.3V，C_L=30pF	10.53	
		V_{DD}=5.0V，C_L=30pF	8.69	
		V_{DD}=5.5V，C_L=30pF	8.44	
High-drive mode, OSPDx<1:0> = 01	T_{Rise}/T_{Fall}	V_{DD}=2.7V，C_L=30pF	3.15	ns
		V_{DD}=3.3V，C_L=30pF	2.63	
		V_{DD}=5.0V，C_L=30pF	2.08	
		V_{DD}=5.5V，C_L=30pF	2.12	
Large current mode, OSPDx<1:0> = 1x	T_{Rise}/T_{Fall}	V_{DD}=2.7V，C_L=30pF	3.17	ns
		V_{DD}=3.3V，C_L=30pF	2.21	
		V_{DD}=5.0V，C_L=30pF	1.54	
		V_{DD}=5.5V，C_L=30pF	1.51	

(1) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(2) Value guaranteed by design, not 100% tested in production.

(3) The data is for reference only, and the specific values are related to PCB Layout.

4.17. Internal reference voltage characteristics

Table 4-27. Internal reference voltage characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	-40 °C < T_J < +105 °C	1.1	1.2	1.3	V
$t_{S\_VREFINT}$(2)(3)	ADC sampling time when reading the internal reference voltage	—	5	—	—	μs
$t_{STA\_VREFINT}$(2)	Start time of V_{REFINT} circuit when ADC is enable	—	—	2	2.5	μs
$I_{DD(VREFINT\_CIR)}$(2)	V_{REFINT} circuit consumption from V_{DD} when converted by ADC	V_{DD} = V_{DDA} = 5.0 V	—	6.5	8	μA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	—	—	4	11	mV
T_{Coeff}(2)	Average temperature coefficient	-40 °C < T_A < +105 °C	—	20	55	ppm/°C

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{DDcoeff}$(2)	Average Voltage coefficient	2.7 V ≤ VDD ≤ 5.5 V	—	110	350	ppm/V

(1) V_{REFINT} is internally connected to the ADC2_IN11 input channel.
(2) Value guaranteed by design, not 100% tested in production.
(3) The shortest sampling time can be determined in the application by multiple iterations.

Table 4-28. Internal reference voltage calibration values

Symbol	Test conditions	Memory address
V_{REFINT}	V_{DD} = V_{DDA} = V_{REFP} = 5.0 V (± 10 mV), Temperature = 25 °C (± 5 °C)	0x1FFF F7FC

4.18. Temperature sensor characteristics

Table 4-29. Temperature sensor characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_L	VSENSE linearity with temperature	T_J = -40 °C to +125 °C	—	±2	—	°C
Avg_Slope	Average slope	—	—	-3.2	—	mV/°C
V_{-40}	Uncalibrated Offset	T_J = -40 °C	—	1.641	—	V
V_{105}	Uncalibrated Offset	T_J = 105 °C	—	1.179	—	V
t_{S_temp}(2)	ADC sampling time when reading the temperature	—	3	—	—	µs
t_{ST_RUN}	Start-up time in Run mode (start-up of buffer)	—	—	1.4	2	
$I_{IDD(TS)}$	Temperature sensor consumption from VDD, when selected by ADC	—	—	25	30	uA

(1) Value guaranteed by design, not 100% tested in production.
(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-30. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1(1)	Temperature sensor raw data acquired value at -40 °C (± 3 °C), V_{DD} = V_{DDA}/V_{REFP} = 5.0V (± 2.0025 mV)	0x1FFF F7D8
TS_CAL2(1)	Temperature sensor raw data acquired value at 105 °C (± 3 °C), V_{DD} = V_{DDA}/V_{REFP} = 5.0V (± 2.0025 mV)	0x1FFF F7FA

(1) TS_CAL use the high 16-bit address.

4.19. ADC characteristics

Table 4-31. ADC characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}/ V_{REFP}	Operating voltage	—	2.7	5	5.5	V
V_{REFN}	Negative Reference Voltage	—	—	V_{SSA}	—	V
f_{ADC}	ADC clock	V_{DDA}/V_{REFP} = 2.7 V to 4.5 V	—	—	30	MHz
		V_{DDA}/V_{REFP} = 4.5 V to 5.5 V	—	—	36	MHz
f_S	Sampling rate	12-bit	—	—	2.4	MSPS
		10-bit	—	—	2.76	
		8-bit	—	—	3.27	
		6-bit	—	—	4	
V_{AIN}	Analog input voltage	17 external; 2 internal	0	—	V_{DDA}/V_{REFP}	V
R_{AIN}	External input impedance	See ***Equation 1***	—	—	90.9	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.5	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	2.9	—	pF
t_s	Sampling time	f_{ADC} = 36 MHz	0.069	—	7.09	μs
t_{CONV}	Total conversion time(including sampling time)	12-bit	—	15	—	1 / f_{ADC}
		10-bit	—	13	—	
		8-bit	—	11	—	
		6-bit	—	9	—	
t_{ST}	Startup time	—	—	—	1	μs
$I_{DDA (ADC)}$	ADC consumption on V_{DDA}/V_{REFP}	f_{ADC} = 36 MHz, V_{DDA}/V_{REFP} = 5 V	—	1.33	—	mA

(1) Value guaranteed by design, not 100% tested in production.

Equation 1:

R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-32. ADC R_{AIN} max for f_{ADC} = 36 MHz(1)(2)

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
2.5	0.069	0.39
7.5	0.208	2.18
13.5	0.375	4.33
28.5	0.791	9.69
41.5	1.15	14.35
55.5	1.54	19.36

T_s (cycles)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
71.5	1.98	25.08
255.5	7.09	90.92

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-33. ADC dynamic accuracy at f_{ADC} = 36 MHz (1)(2)(3)(4)

Symbol	Description	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz V_{DDA}/V_{REFP} = 5.0 V Input Frequency = 20 kHz Temperature = 25 °C	Channel-dedicated sample-and-hold circuits in use	TBD	10.55	—	bits
			Channel-dedicated sample-and-hold circuits not in use	TBD	11.13	—	
SNDR	Signal-to-noise and distortion ratio		Channel-dedicated sample-and-hold circuits in use	TBD	65.22	—	dB
			Channel-dedicated sample-and-hold circuits not in use	TBD	63.00	—	
SNR	Signal-to-noise ratio		Channel-dedicated sample-and-hold circuits in use	TBD	65.31	—	
			Channel-dedicated sample-and-hold circuits not in use	TBD	69.03	—	
THD	Total harmonic distortion		Channel-dedicated sample-and-hold circuits in use	—	-81.33	TBD	
			Channel-dedicated sample-and-hold circuits not in use	—	-80.26	TBD	

(1) Value guaranteed by sample, not 100% tested in production.

(2) When the sample-and-hold circuit is working, the ADC input voltage ranges from (0.2V) to (V_{DD} -0.2V).

(3) Results for LQFP64 packages. The values for other packages might differ.

(4) System clock = 180MHz, PCLK2 = 180MHz, System clock from HXTAL, ADC_CLK from PCLK2.

Table 4-34. ADC static accuracy at f_{ADC} = 36 MHz (1)(2)(3)(4)

Symbol	Description	Test conditions		Min	Typ	Max	Unit
EO	Offset error	f_{ADC} = 36 MHz V_{DDA}/V_{REFP} = 5.0 V Input Frequency = 1 kHz Temperature = 25 °C	Channel-dedicated sample-and-hold circuits in use	TBD	1.5	—	LSB
			Channel-dedicated sample-and-hold circuits not in use	TBD	1.5	—	

Symbol	Description	Test conditions		Min	Typ	Max	Unit
DNL	Differential linearity error		Channel-dedicated sample-and-hold circuits in use	TBD	0.8	—	
			Channel-dedicated sample-and-hold circuits not in use	TBD	0.8	—	
INL	Integral linearity error		Channel-dedicated sample-and-hold circuits in use	TBD	-1.67	—	
			Channel-dedicated sample-and-hold circuits not in use	TBD	-1.67	—	

(1) Value guaranteed by sample, not 100% tested in production.

(2) When the sample-and-hold circuit is working, the ADC input voltage ranges from (0.2V) to (V_{DD} -0.2V).

(3) Results for LQFP64 packages. The values for other packages might differ.

(4) System clock = 180MHz, PCLK2 = 180MHz, System clock from HXTAL, ADC_CLK from PCLK2.

Figure 4-12. Differential linearity error

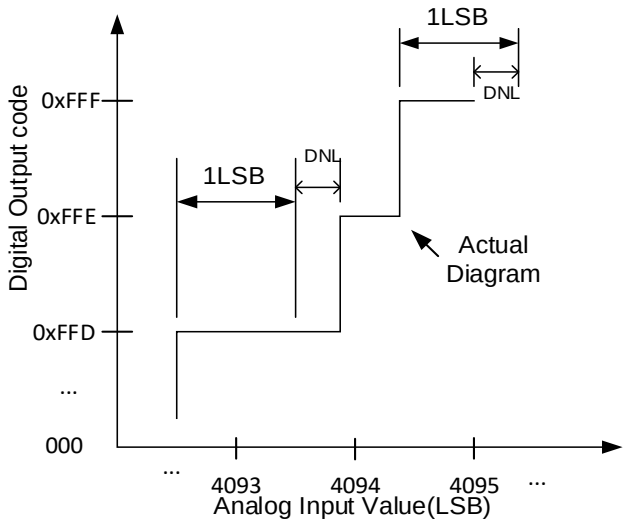
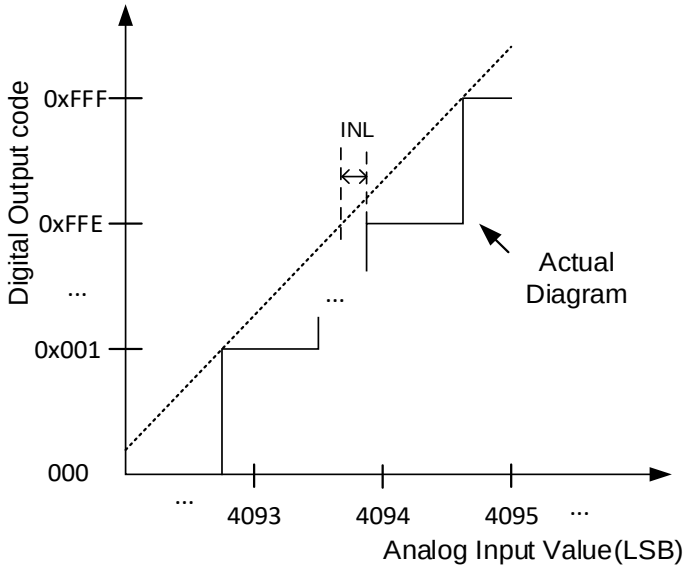


Figure 4-13. Integral linearity error



4.20. POC characteristics

Table 4-35. POC Timing(1)

Symbol	Description		Conditions	Min	Typ	Max	Unit
t_{POCW}	POCn# input pulse width (n=0,1…5)		See ***Figure 4-14***	1.5	—	—	t_{hcyc}
t_{POCDI}	Output disable time	Transition of the POCn# signal level	See ***Figure 4-15*** ,When detecting falling edges (POC_INDCFGn.DMDSEL[3:0] = 0000 (n = 0…12))	—	3hclk	—	μs
t_{POCDO}		Simultaneous conduction of output pins	See ***Figure 4-16***	—	2hclk	—	μs
t_{POCDC}		Detection of comparator outputs	See ***Figure 4-17*** ,The time is that when the noise filter for comparator C is not in use (CMP0_CS. CMP0DFSCDIV[1:0] = 00) and excludes the time for detection by comparator C.	—	3hclk	—	μs
t_{POCDS}		Register setting	See ***Figure 4-18*** ,Time for access to the register is not included.	—	2hclk	—	μs
t_{POCDOS}		Oscillation stop detection	See ***Figure 4-19***	—	3hclk	—	μs
t_{LOUP}	CPU Lockup		—	—	2hclk	—	μs

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-14. POC Input Timing

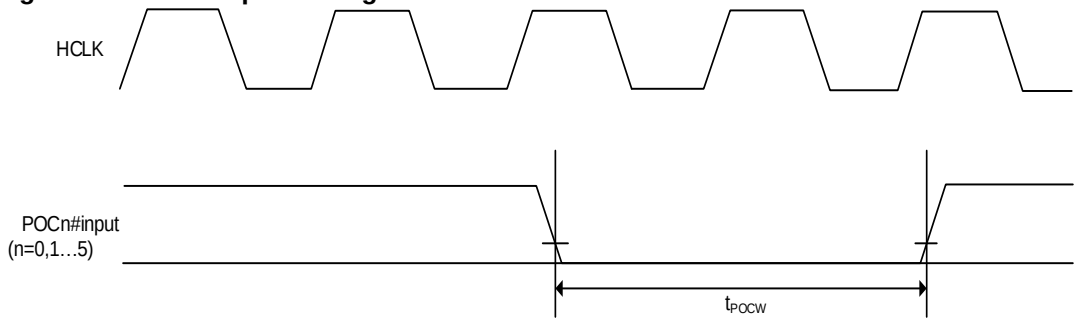


Figure 4-15. Output Disable Time for POC in Response to Transition of the POCn# Signal Level

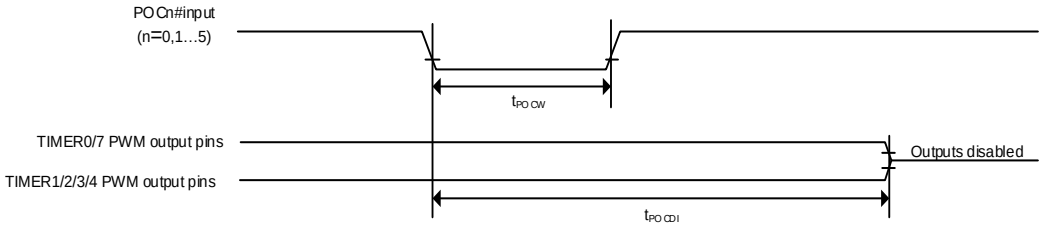


Figure 4-16. Output Disable Time for POC in Response to the Simultaneous Conduction of Output Pins

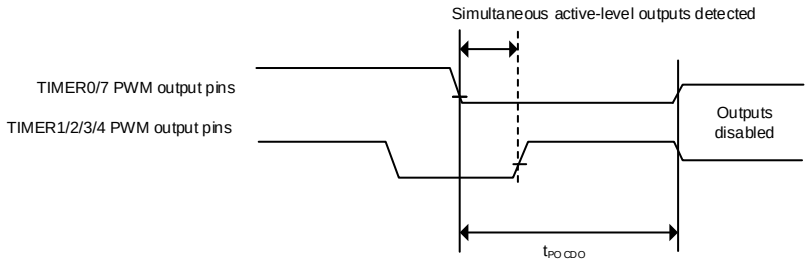


Figure 4-17. Output Disable Time for POC in Response to Detection of the Comparator Outputs

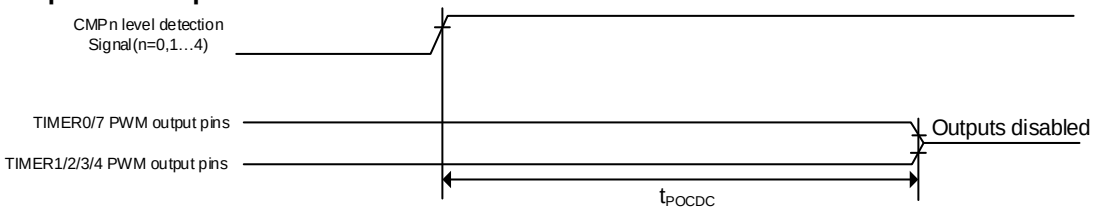


Figure 4-18. Output Disable Time for POC in Response to the Register Setting

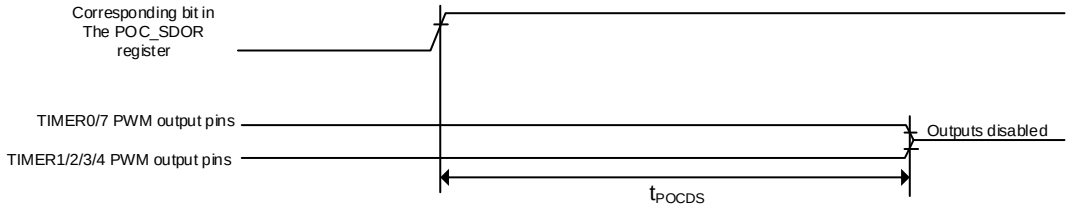
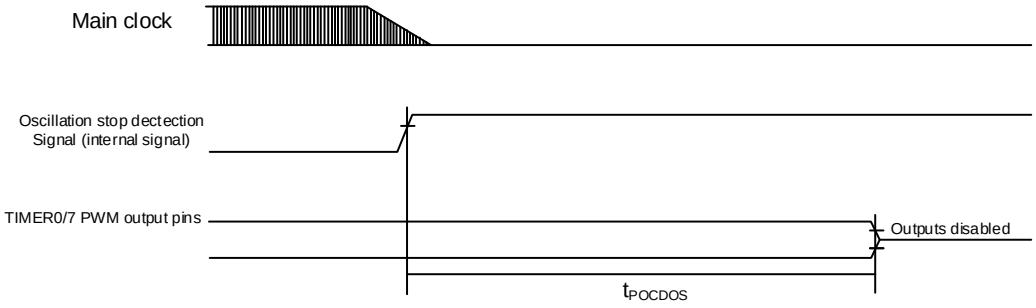


Figure 4-19. Output Disable Time for POC in Response to the the Oscillation Stop Detection



4.21. GTOC characteristics

Table 4-36. GTOC Timing(1)

Symbol	Description		Conditions	Min	Typ	Max	Unit
T_{GTOCW}	GTOCn input pulse width (n = A to D)		See ***Figure 4-20***	1.5	—	—	t_{PBcyc}
t_{GTOCDI}	Output disable time	Input level detection of the GTOCn pin (via flag)	See ***Figure 4-21*** When the digital noise filter is not in use (GTOC_CFGx.NFEN = 0 (x=0…3))	—	5hclk	—	μs
t_{GTOCDE}		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	See ***Figure 4-22***	—	5hclk	—	μs
t_{GTOCDC}		Edge detection signal from a comparator	See ***Figure 4-23*** The time is that when the noise filter for comparator is not in use (CMPn_CS.CMPnDFSCDIV[1:0] = 00 (n=0…3)) and excludes the time for detection by comparator.	—	5hclk	—	μs
t_{GTOCDS}		Register setting	See ***Figure 4-24*** Time for access to the register is not included.	—	4hclk	—	μs
$t_{GTOCDOS}$		Oscillation stop detection	See ***Figure 4-25***	—	5hclk	—	μs
$t_{GTOCDDI}$		Input level detection of the GTOCn pin (direct path)	See ***Figure 4-26***	—	5hclk	—	μs
$t_{GTOCDDC}$		Level detection signal from a comparator	See ***Figure 4-27*** The time is that when the noise filter for comparator C is not in use (CMPn_CS.CMPnDFSCDIV[1:0] = 00 (n=0…3)) and excludes the time for detection by comparator.	—	5hclk	—	μs
t_{LOUP}	CPU Lockup		—	—	4hclk	—	μs

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-20. GTOC Input Timing

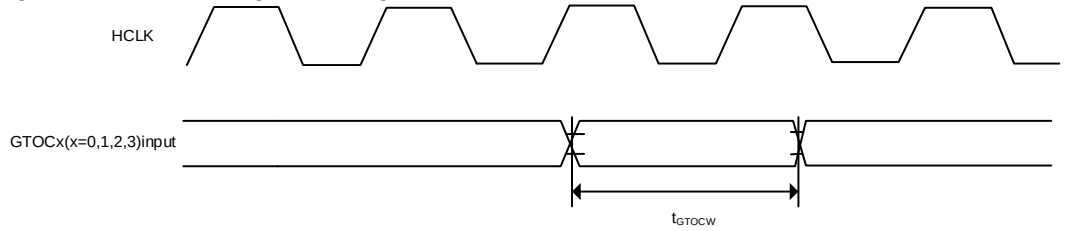


Figure 4-21. Output Disable Time for GTOC via Detection Flag in Response to the Input Level Detection of the GTOCx(x=0,1,2,3) pin

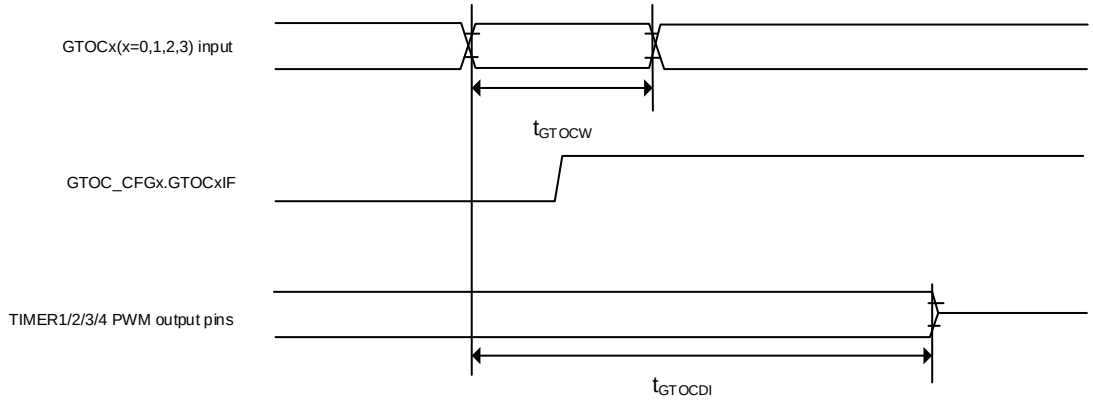


Figure 4-22. Output Disable Time for GTOC in Response to Detection of the Output Stopping Signal from TIMER1/2/3/4

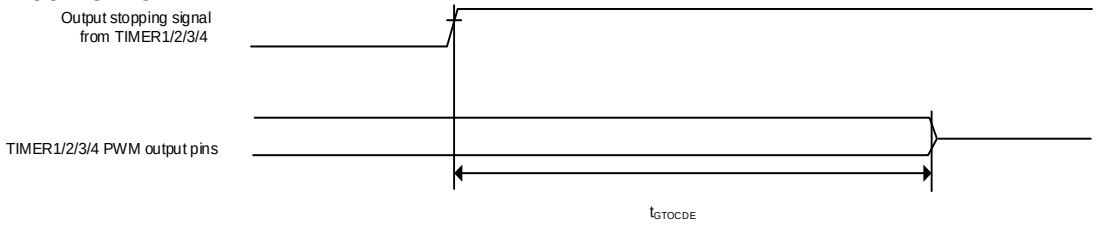


Figure 4-23. Output Disable Time for GTOC in Response to Edge Detection Signal from a Comparator

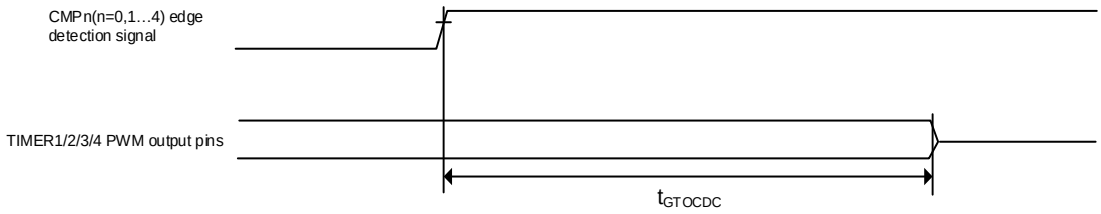


Figure 4-24. Output Disable Time for GTOC in Response to the Register Setting

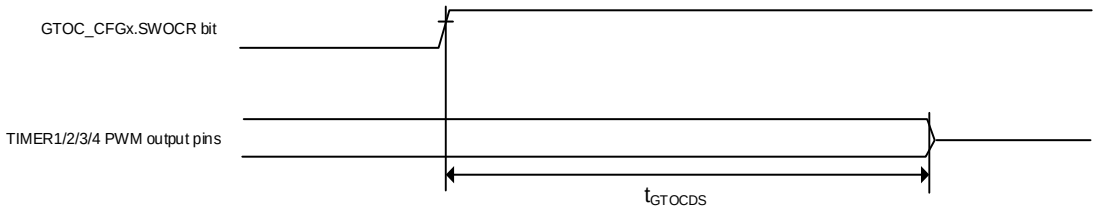


Figure 4-25. Output Disable Time of GTOC in Response to the Oscillation Stop

Detection

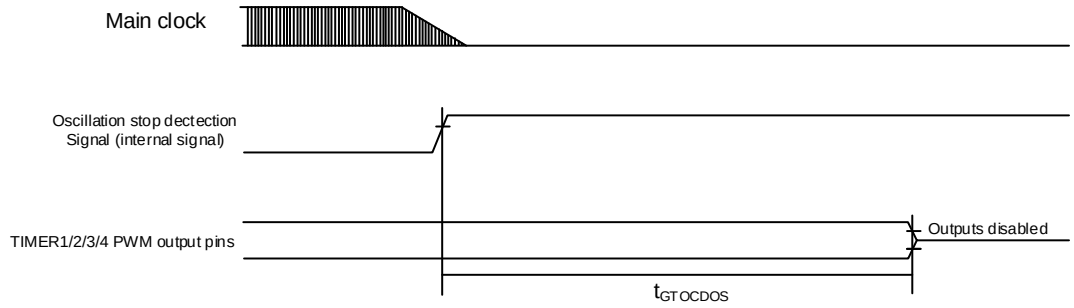


Figure 4-26. Output Disable Time for GTOC in Direct Response to the Input Level Detection of the GTOCx(x=0,1,2,3) pin

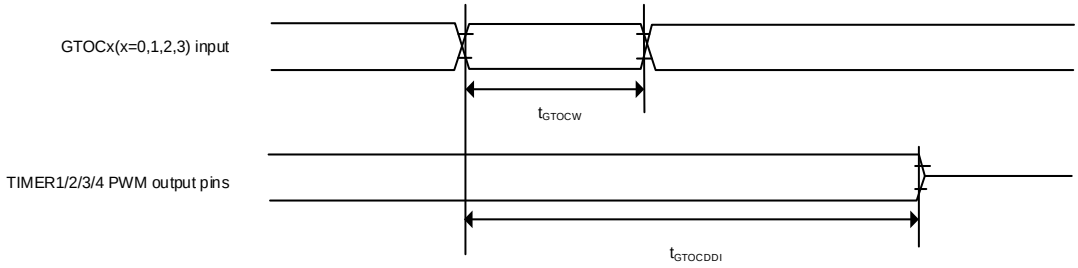
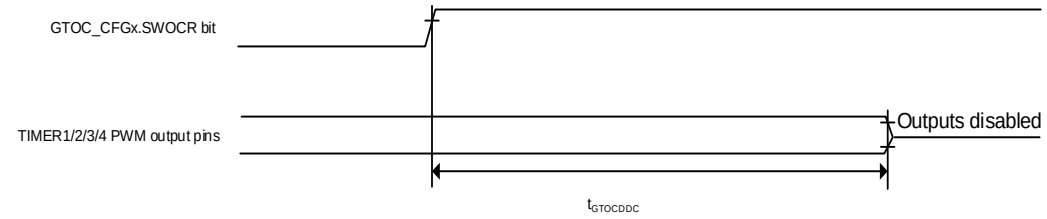


Figure 4-27. Output Disable Time for GTOC in Response to Level Detection Signal from a Comparator



4.22. DAC characteristics

Table 4-37. DAC characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA2}/ V_{REFP2}	Operating voltage	—	2.7	5	5.5	V
V_R	Resolution	—	—	12	—	Bit
R_{LOAD}	Load resistance	Resistive load	2	—	—	MΩ
Ro	Impedance output	—	—	5.7	—	kΩ
C_{LOAD}	Load capacitance	No pin/pad capacitance included	—	—	20	pF
DAC_OUT min	Lower DAC_OUT voltage	—	0	—	—	mV
DAC_OUT max	Higher DAC_OUT voltage	—	—	—	V_{DDA2}/ V_{REFP2}	V
$I_{DDA/REFP}$	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, VDDA2/VREFP2 = 5.0 V	—	226.3	—	uA
		With no load, worst code(0xAAB) on the input, VDDA2/VREFP2 = 5.0 V	—	295.6	—	uA
$T_{SETTING}$	Settling time(full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±1LSB)	C_{LOAD} =20 pF	—	1.92	—	μs
T_{WAKEUP}	Wakeup from off state	—	—	—	5	μs
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	C_{LOAD} ≤ 20 pF, R_{LOAD} ≥ 2MΩ	—	—	0.4	MS/s

(1) Value guaranteed by design, not 100% tested in production.

Table 4-38. DAC accuracy(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non-linearity Error	DAC in 12-bit mode	—	0.68	—	LSB
INL	Integral non-linearity	DAC in 12-bit mode	—	1.29	—	LSB
Offset	Offset error	DAC in 12-bit mode	—	1.87	—	LSB
GE	Gain error	DAC in 12-bit mode	—	0.03	—	%

(1) Value guaranteed by sample, not 100% tested in production.

4.23. Comparators characteristics

Table 4-39. CMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}/V_{REFP}	Operating voltage	—	2.7	5	5.5	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}/V_{REFP}	V
t_D(2)	Propagation delay for 200mV step with 100 mV overdrive	—	—	48.95	—	ns
	Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs	—	—	56.65	—	ns
t_{START}	Comparator startup time to reach propagation delay specification	—	—	—	0.6	μs
$I_{DDA/REFP(CMP)}$	Current consumption from V_{DDA}/V_{REFP}	Static	—	71	83	μA
		With 50 kHz ±100 mV overdrive square signal	—	68	78	
V_{offset}	Offset error	—	—	±5	—	mV
V_{hyst}	Hysteresis Voltage	No Hysteresis	—	0	—	mV
		Low Hysteresis	—	16	—	
		Medium Hysteresis	—	32	—	
		High Hysteresis	—	50	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by sample, not 100% tested in production.

4.24. Trigonometric Math Unit (TMU) characteristics

The TMU unit has 5 different operation modes.

Table 4-40. TMU supported instructions characteristics(1)

Mode Number	Operation	Cycles(max)
1	$R0 = \sqrt{x}$	4
2	$R0 = \sin(x)$	7
3	$R0 = \cos(x)$	7
4	$R0 = \arctan(x)$	7
5	$R0 = \sqrt{x^2+y^2}$	7

(1) Value guaranteed by design, not 100% tested in production.

4.25. I2C characteristics

Table 4-41. I2C characteristics(1)(2)

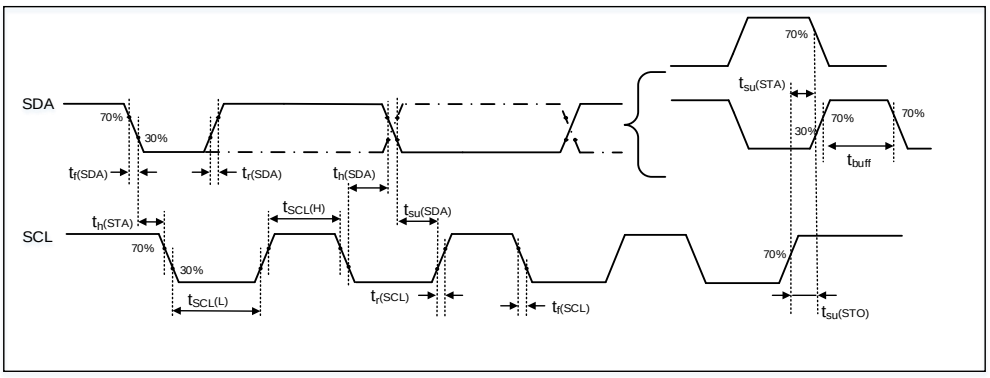
Symbol	Description	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0(3)	3450	0(3)	900	0	450	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{su(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{su(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-28. I2C bus timing diagram



4.26. SPI characteristics

Table 4-42. Standard SPI characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	22.5	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLK2} = 180MHz, presc = 4	—	22.3	—	ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLK2} = 180 MHz, presc = 4	—	22.3	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	8.57	ns
$t_{SU(MI)}$	Data input setup time	—	3	—	—	ns
$t_{H(MI)}$	Data input hold time	—	2	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	3	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	2	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	20	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	5	—	ns
$t_{V(SO)}$	Data output valid time	—	—	12.5	—	ns
$t_{SU(SI)}$	Data input setup time	—	1	—	—	ns
$t_{H(SI)}$	Data input hold time	—	2	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-29. SPI timing diagram - master mode

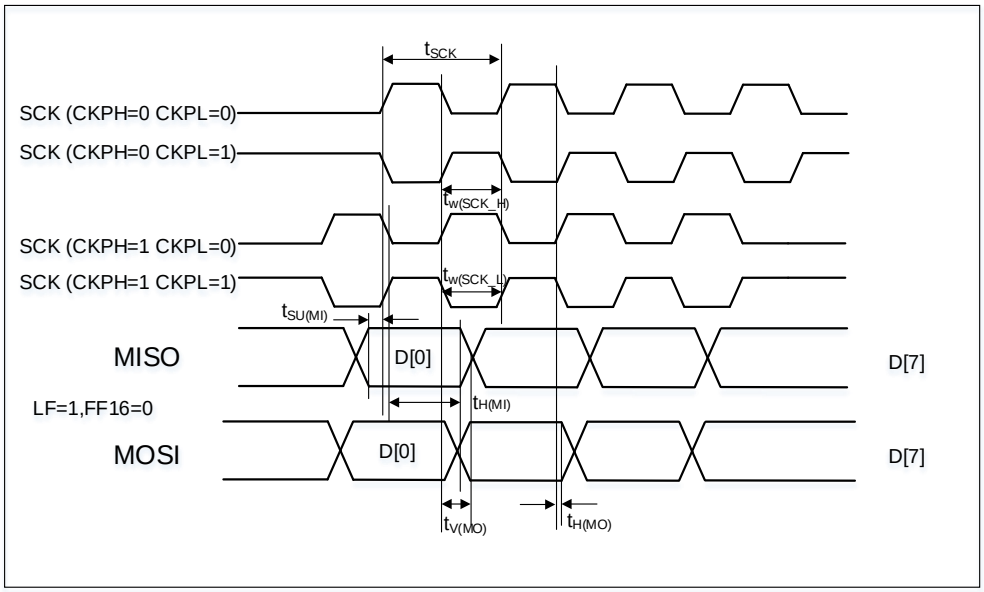


Figure 4-30. SPI timing diagram - slave mode(CKPH=0)

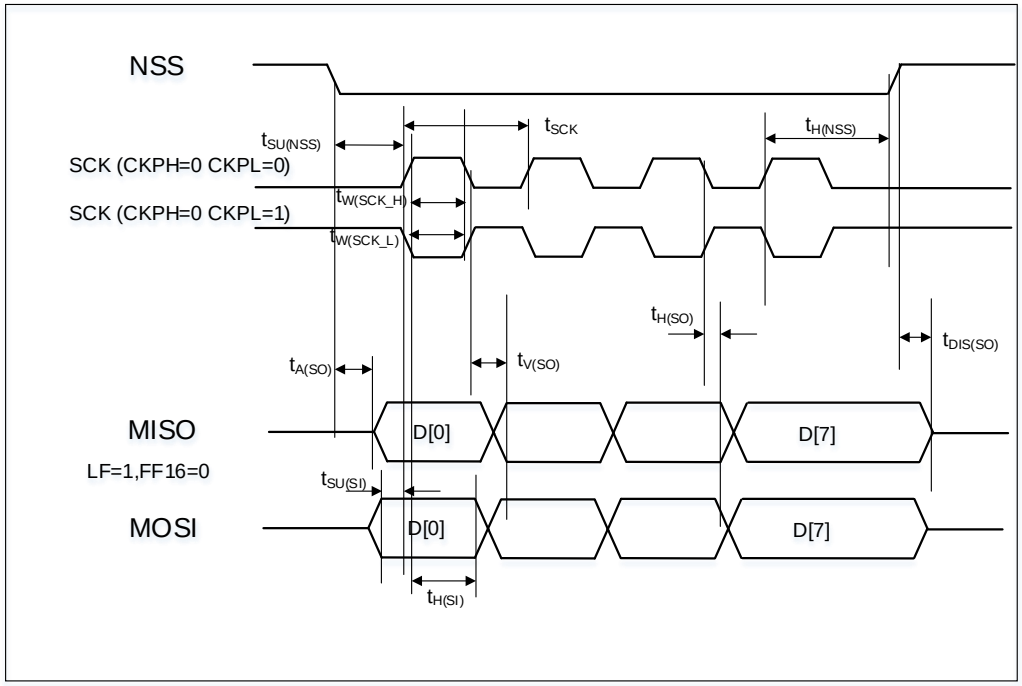
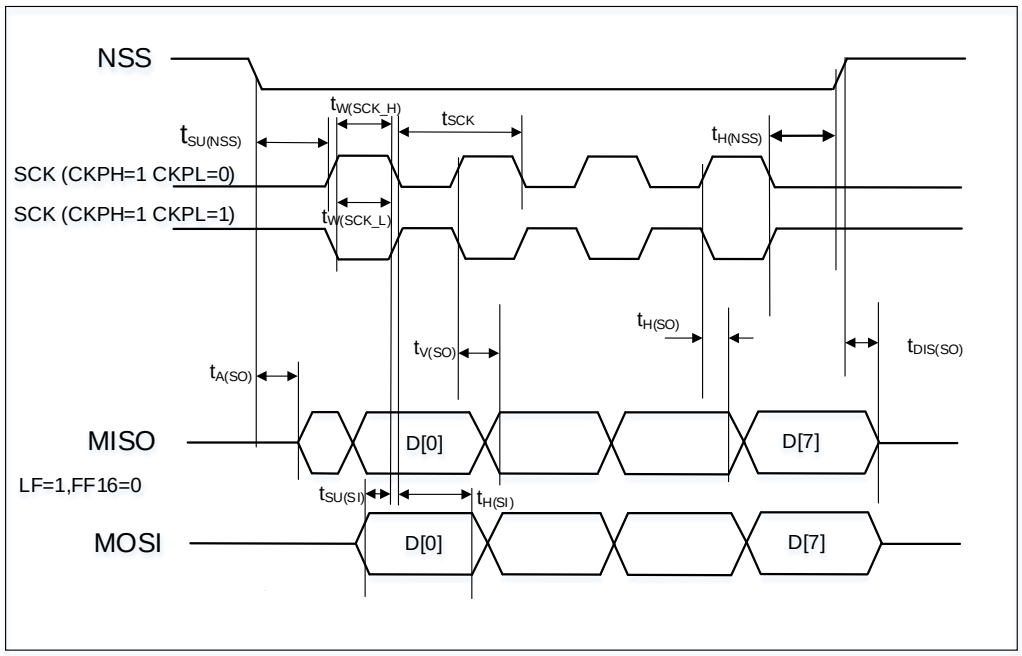


Figure 4-31. SPI timing diagram - slave mode(CKPH=1)



4.27. UART characteristics

Table 4-43. UART characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	f_{PCLK1} = 90 MHz	—	—	45	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLK1} = 90 MHz	5.6	—	—	ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLK1} = 90 MHz	5.6	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.28. CAN characteristics

Table 4-44. CAN characteristics(1) (2)

Symbol	Description	Conditions	Min(2)	Typ(1)	Max(2)	Unit
Classic CAN mode	Bit rate for communications	—	—	0.5	1	Mbps

(1) Value guaranteed by design, not 100% tested in production.

(2) To get more about the I/O alternate function characteristics (CAN TX and CAN RX), see ***Table 4-24. I/O static characteristics***.

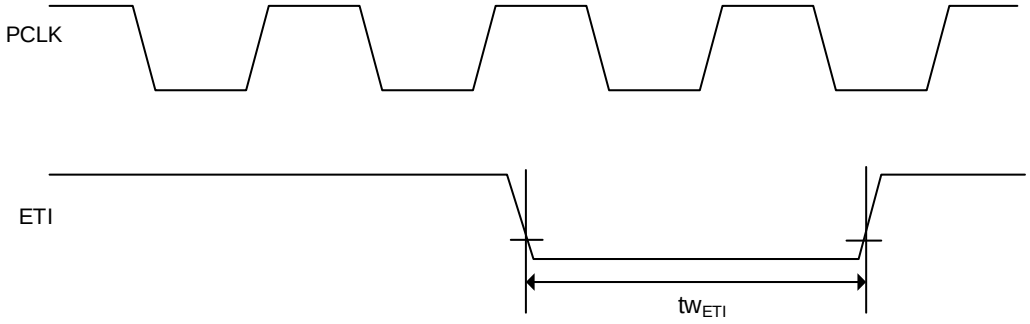
4.29. TIMER characteristics

Table 4-45. TIMER characteristics(1)

Symbol	Description	Conditions	Min	Max	Unit
t_{RES}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	5.56	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}$ /2	MHz
		$f_{TIMERxCLK}$ = 180 MHz	0	90	MHz
tw_{ETI}	External trigger input pulse width	See ***Figure 4-32***	2	—	t_{PBcyc}
RES	Timer resolution	TIMERx	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180MHz	0.00556	364.1	μs
t_{MAX_COUNT}	Maximum possible count	—	—	65536* 65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	—	23.86	s

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-32. TIMER External Trigger Input Timing



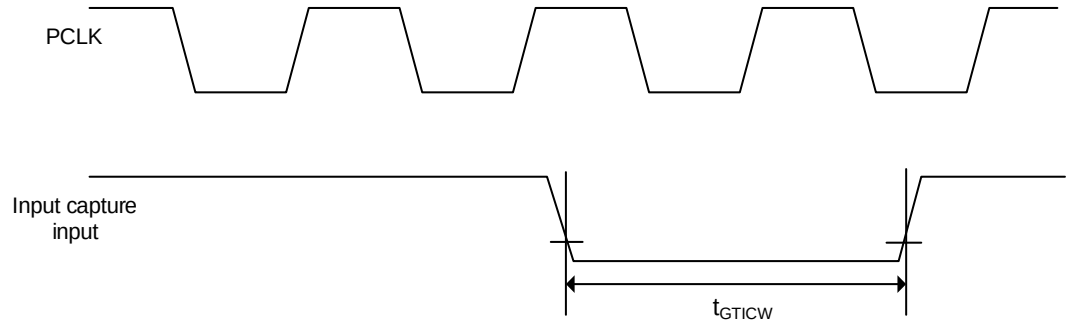
4.30. GPTIMER characteristics

Table 4-46. GPTIMER characteristics(1)

Symbol	Description		Conditions	Min	Max	Unit
t_{RES}	GPTimer resolution time		—	1	—	$t_{TIMERxCLK}$
			$f_{TIMERxCLK}$ = 180 MHz	5.56	—	ns
f_{EXT}	GPTimer external clock frequency		—	0	$f_{TIMERxCLK}$ /2	MHz
			$f_{TIMERxCLK}$ = 180 MHz	0	90	MHz
t_{GTICW}	Input capture input pulse width	Single-edge setting	See Figure 4-33	1.5	—	t_{PCLK}
		Both-edge setting		2.5	—	
RES	GPTimer resolution		GPTIMERx	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		—	1	65536	$t_{TIMERxCLK}$
			$f_{TIMERxCLK}$ = 180 MHz	0.00556	364.1	µs
t_{MAX_COUNT}	Maximum possible count		—	—	65536* 65536	$t_{TIMERxCLK}$
			$f_{TIMERxCLK}$ = 180 MHz	—	23.86	s

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-33. GPTIMER External Trigger Input Timing



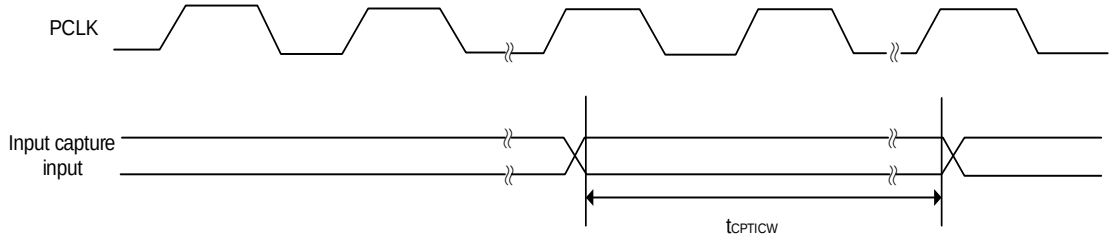
4.31. Compare TIMER characteristics

Table 4-47. CPTIMER characteristics(1)

Symbol	Description		Conditions	Min	Max	Unit
t_{RES}	CPTimer resolution time		—	1	—	$t_{CPxTIMERCLK}$
			$f_{CPxTIMERCLK}$ = 90 MHz	11.11	—	ns
t_{CPTICW}	Input capture input pulse width	Single-edge setting	See *Figure 4-34*	1.5	—	$t_{CPxTIMERCLK}$
		Both-edge setting		2.5	—	
RES	CPTimer resolution		—	—	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		—	1	65536	$t_{CPxTIMERCLK}$
			$f_{CPxTIMERCLK}$ = 90 MHz	11.11	728.1	μs
t_{MAX_COUNT}	Maximum possible count (CPTimer)		—	—	65536* 65536	$t_{CPxTIMERCLK}$
			$f_{CPxTIMERCLK}$ = 90 MHz	—	47.72	s

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-34. Compare TIMER Input Capture Input Timing



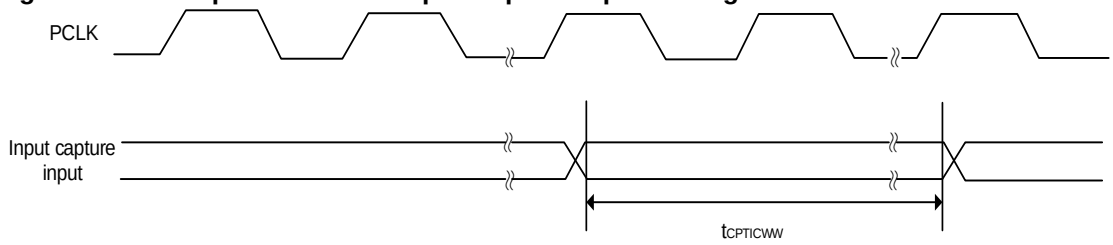
4.32. Compare TIMER W characteristics

Table 4-48. CPTIMER W characteristics(1)

Symbol	Description		Conditions	Min	Max	Unit
t_{RES}	CPTimer W resolution time		—	1	—	$t_{CPxTIMERWCLK}$
			$f_{CPxTIMERWCLK}$ = 90 MHz	11.11	—	ns
t_{CPTICW}	Input capture input pulse width	Single-edge setting	See *Figure 4-35*	1.5	—	$t_{CPxTIMERWCLK}$
		Both-edge setting		2.5	—	
RES	CPTimer W resolution		—	—	32	bit
$t_{COUNTER}$	32-bit counter clock period when internal clock is selected		—	1	65536* 65536	$t_{CPxTIMERWCLK}$
			$f_{CPxTIMERWCLK}$ = 90 MHz	11.11	47.72	s
t_{MAX_COUNT}	Maximum possible count (CPTimer W)		—	—	65536* 65536* 65536	$t_{CPxTIMERWCLK}$
			$f_{CPxTIMERWCLK}$ = 90 MHz	—	868.72	h

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-35. Compare TIMER W Input Capture Input Timing



4.33. WWDGT characteristics

Table 4-49. WWDGT min-max timeout value at 90 MHz (fPCLK1)(1)

Prescaler divider	PSC[1:0] bits	Min timeout value CNT[13:0] =0x01	Unit	Max timeout value CNT[13:0]=0x3FFF	Unit
1/1	00	45.5	µs	745.6	ms
1/2	01	91.0		1491.2	
1/4	10	182.0		2982.4	
1/8	11	364.1		5964.9	

(1) Value guaranteed by design, not 100% tested in production.

4.34. FWDGT characteristics

Table 4-50. FWDGT min/max timeout period at 32 kHz (IRC32K)(1)

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x001	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.125	511.875	ms
1/8	001	0.256	1048.32	
1/16	010	0.512	2096.64	
1/32	011	1.024	4193.28	
1/64	100	2.048	8386.56	
1/128	101	4.096	16773.12	
1/256	110 or 111	8.192	33546.24	

(1) Value guaranteed by design, not 100% tested in production.

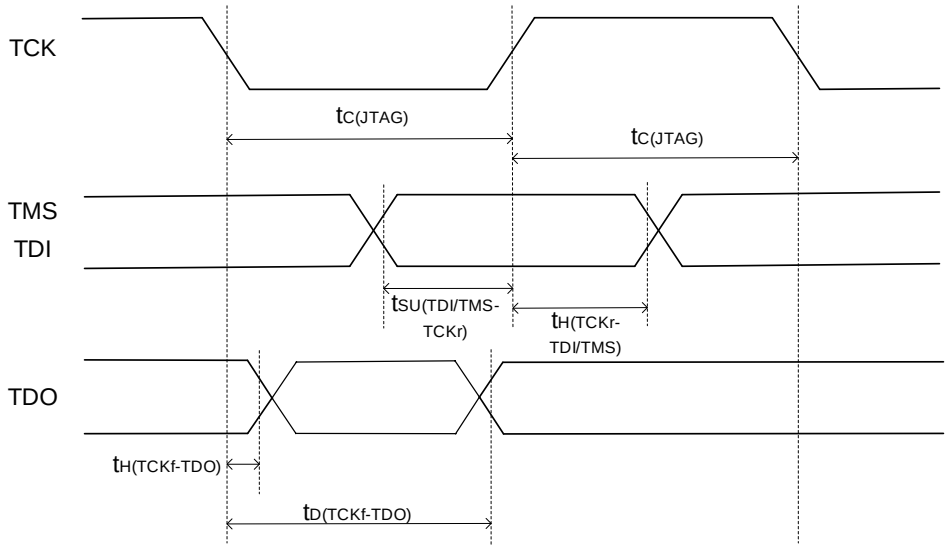
4.35. JTAG Timing

Table 4-51. JTAG Scan Interface Timing (1)

Symbol	Description	Min	Max	Unit
$t_{C(JTAG)}$	Cycle time, JTAG low and high period	20.8	—	ns
$t_{SU(TDI/TMS - TCKr)}$	Setup time, TDI, TMS before TCK rise (TCKr)	8	—	ns
$t_{H(TCKr -TDI/TMS)}$	Hold time, TDI, TMS after TCKr	1	—	ns
$t_{H(TCKf -TDO)}$	Hold time, TDO after TCKf	7	—	ns
$t_{D(TCKf -TDO)}$	Delay time, TDO valid after TCK fall (TCKf)	—	7.5	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-36. JTAG timing diagram



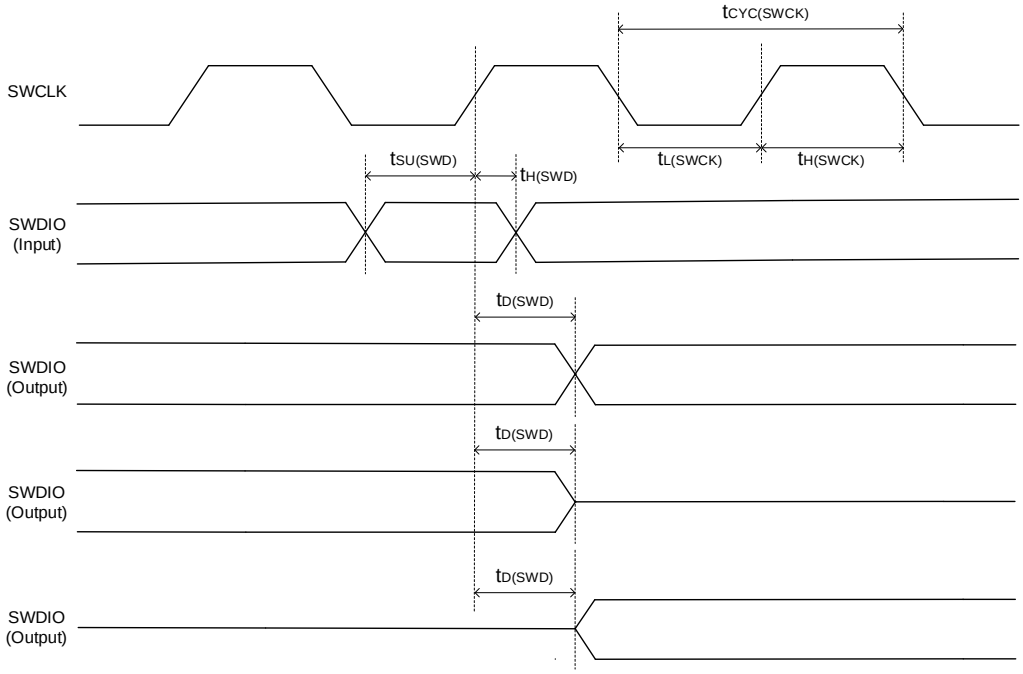
4.36. SWD Timing

Table 4-52. SWD Interface Timing (1)

Symbol	Description	Min	Max	Unit
$t_{CYC(SWCK)}$	SWCLK clock cycle time	20.8	—	ns
$t_{H(SWCK)}$	SWCLK clock high pulse width	10	—	ns
$t_{L(SWCK)}$	SWCLK clock low pulse width	10	—	ns
$t_{R(SWCK)}$	SWCLK clock rise time	—	1	ns
$t_{F(SWCK)}$	SWCLK clock fall time	—	1	ns
$t_{SU(SWD)}$	SWDIO setup time	8	—	ns
$t_{H(SWD)}$	SWDIO hold time	1	—	ns
$t_{D(SWD)}$	SWDIO data delay time	7	7.5	ns

(1) Guaranteed by design, not 100% tested in production

Figure 4-37. SWD timing diagram



5. Package information

5.1. LQFP64 package outline dimensions

Figure 5-1. LQFP64 package outline

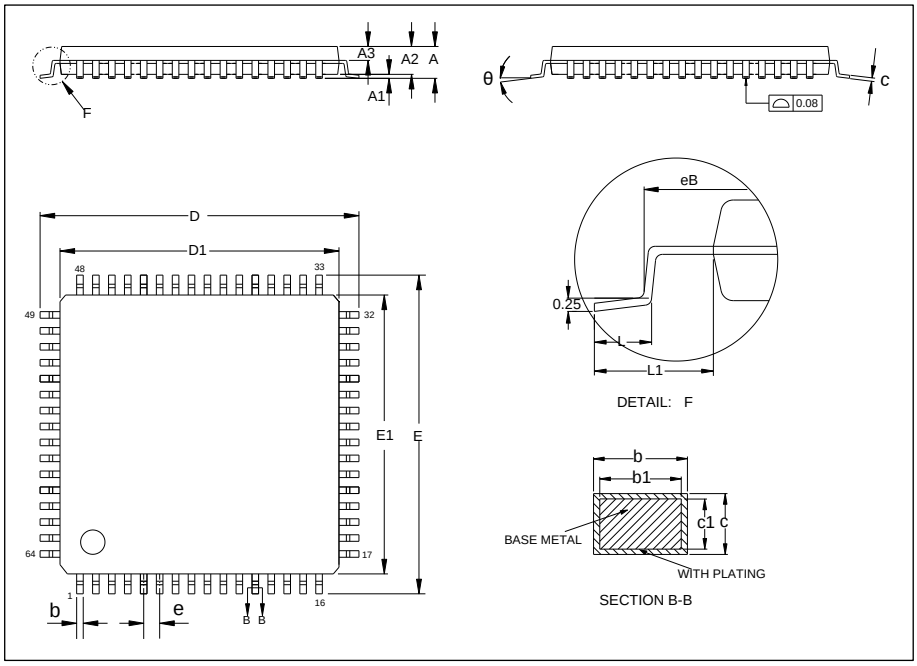
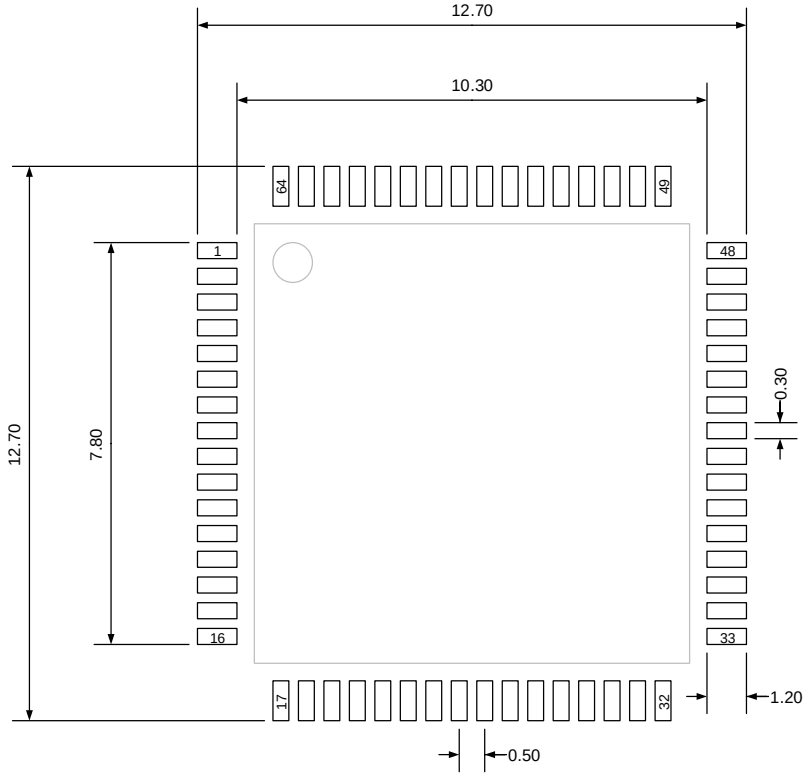


Table 5-1. LQFP64 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	—	0.50	—
eB	11.25	—	11.45
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP48 package outline dimensions

Figure 5-3. LQFP48 package outline

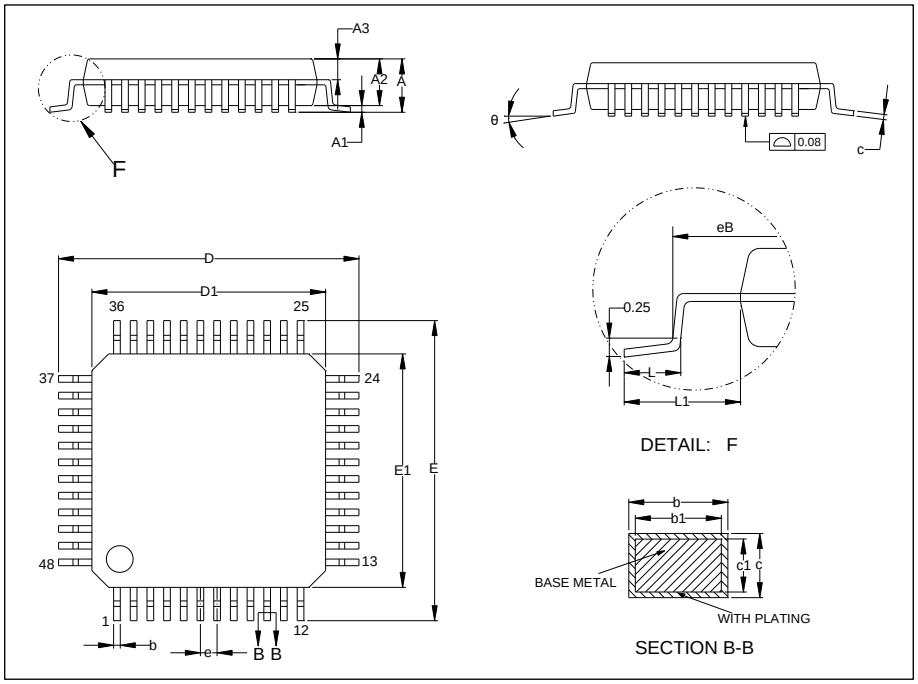
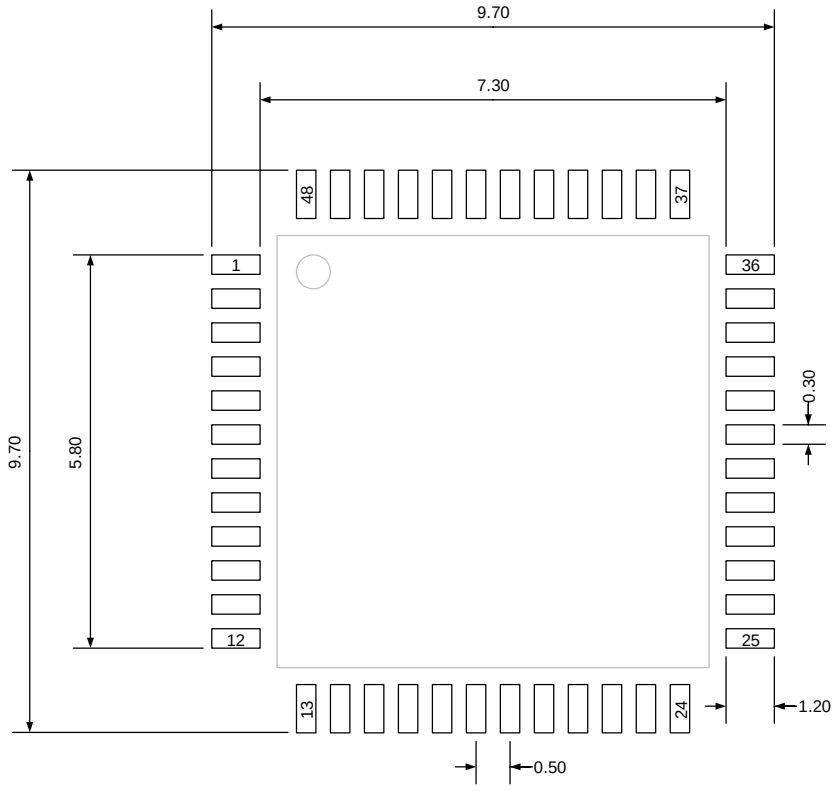


Table 5-2. LQFP48 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	—	0.50	—
eB	8.10	—	8.25
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-4. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.3. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-3. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP64	51.81	°C/W
		LQFP48	64.40	
θ_{JB}	Cold plate, 2S2P PCB	LQFP64	33.36	°C/W
		LQFP48	42.32	
θ_{JC}	Cold plate, 2S2P PCB	LQFP64	11.25	°C/W
		LQFP48	22.47	

Symbol	Condition	Package	Value	Unit
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP64	33.53	°C/W
		LQFP48	42.42	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP64	0.49	°C/W
		LQFP48	1.74	

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32M531xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32M531RCT7	256	LQFP64	Green	Industrial -40 °C to +105 °C
GD32M531RZT7	196	LQFP64	Green	Industrial -40 °C to +105 °C
GD32M531RBT7	128	LQFP64	Green	Industrial -40 °C to +105 °C
GD32M531CCT7	256	LQFP48	Green	Industrial -40 °C to +105 °C
GD32M531CZT7	196	LQFP48	Green	Industrial -40 °C to +105 °C
GD32M531CBT7	128	LQFP48	Green	Industrial -40 °C to +105 °C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.6, 2026

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